UNITED STATES DISTRICT COURT

FOR THE WESTERN DISTRICT OF TEXAS

MIDLAND/ODESSA DIVISION

REDSTONE LOGICS LLC, Plaintiff, v. MEDIATEK, INC. and MEDIATEK USA, INC., Defendants.	Case No. 7:24-cv-00029-DC-DTG

DECLARATION OF R. JACOB BAKER, Ph.D., P.E., IN SUPPORT OF DEFENDANTS' OPENING CLAIM CONSTRUCTION BRIEF

I. INTRODUCTION

1. My name is R. Jacob Baker, Ph.D., P.E., and I am an Emeritus Professor of Electrical and Computer Engineering at the University of Nevada, Las Vegas ("UNLV"). I have prepared this declaration as an expert witness on behalf of Defendants MediaTek, Inc., and MediaTek USA, Inc. In this declaration, I provide my opinions regarding the understanding of a person of ordinary skill in the art ("PHOSITA") with respect to certain claim terms of U.S. Patent No. 8,549,339 ("the '339 Patent").

2. This declaration contains statements of my opinions formed to date, and the bases and rationale for these opinions. I may offer additional opinions based on further review of materials in this case, including opinions and/or testimony of other expert witnesses.

3. In forming my opinions herein, I have relied upon (1) the specification, claims, and file history of the '339 Patent; (2) the materials cited in this declaration; and (3) my background and experience in this field.

4. For my efforts in connection with the preparation of this declaration, I have been compensated at my usual and customary rate for this type of consulting activity. My compensation is in no way contingent on the results of these or any other proceedings related to the '339 Patent.

A. Qualifications / Professional Background

5. My qualifications generally are set forth in my Curriculum Vitae, which is attached as Appendix A, which also includes a list of the publications I have authored and a list of the other cases in which I have testified during the last four years.

6. I have been working as an engineer since 1985, and I have been teaching Electrical and Computer Engineering courses since 1991.

7. I received B.S. and M.S. degrees in Electrical Engineering from UNLV in 1986 and 1988, respectively. I received my Ph.D. in Electrical Engineering from the University of Nevada,

Reno ("UNR"), in 1993.

8. My doctoral research, culminating in the award of a Ph.D., investigated the use of power MOSFETs in the design of very high peak power, and high-speed, instrumentation. I developed techniques to reliably stack power MOSFETs to switch higher voltages, that is, greater than 1,000 V and 100 Amps of current with nanosecond switching times. This work was reported in the paper entitled "Transformerless Capacitive Coupling of Gate Signals for Series Operation of Power MOSFET Devices," published in the IEEE Transactions on Power Electronics. The paper received the Best Paper Award in 2000.

B. Industry Experience

9. From 1985 to 1993, I worked for EG&G Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for underground nuclear weapon tests at the Nevada test site. During this time, I designed, and oversaw the fabrication of, over 30 electronic and electro-optic instruments, including high-speed cable and fiber-optic receiver/transmitters, PLLs, frame and bit-syncs, data converters, streak-camera sweep circuits, Pockel's cell drivers, micro-channel plate gating circuits, charging circuits for battery backup of equipment for recording test data, and analog oscilloscope electronics.

10. My work during this time, as one example, had a direct impact on my doctoral research work using power MOSFETs, subsequent publishing efforts, and industry designs. In addition to the 2000 Best Paper Award from the IEEE Power Electronics Society, I published several other papers in related areas while working in industry. I hold a patent, U.S. Patent No. 5,874,830, in the area of power supply design, titled, "Adaptively Biased Voltage Regulator and Operating Method," which was issued on February 23, 1999. I have designed dozens of linear and switching power supplies for commercial products and scientific instrumentation.

11. I am a licensed Professional Engineer and have extensive industry experience in

circuit design, fabrication, and manufacture of Dynamic Random Access Memory (DRAM) semiconductor integrated circuit chips, Phase-Change Random Access Memory (PCRAM) chips, and CMOS Image Sensors (CISs) at Micron Technology, Inc. ("MTI") in Boise, Idaho. I spent considerable time working on the development of flash memory chips while at MTI. My efforts resulted in more than a dozen patents relating to flash memory. One of my projects at MTI included the development, design, and testing of circuit design techniques for a multi-level cell (MLC) flash memory using signal processing. This effort resulted in higher-density memories for use in solid-state drives and flash memory cards having an ATA interface that are ubiquitous in consumer electronics, including cameras and data storage systems. Further, the use of higher-density memory can result in fewer changes in the flash translation layer for logical-to-physical addressing, less need for garbage collection, and larger data segments that can improve a computing system's performance. Another project I worked on at MTI focused on the design of buffers for high-speed double-data rate DRAM, which resulted in around 10 U.S. patents in buffer design. Among many other experiences, I led the development of the delay locked loop (DLL) in the late 1990s so that MTI DRAM products could transition to the DDR memory protocol, used in mobile and non-mobile (server, desktop, cell phones, tablets, etc.) computing systems as main computer memory, for addressing and controlling accesses to memory via interprocess communications (IPC) with the memory controller (MC). I provided technical assistance with MTI's acquisition of Photobit during 2001 and 2002, including transitioning the manufacture of CIS products into MTI's process technology. Further, I did consulting work at Sun Microsystems and then Oracle on the design of memory modules during 2009 and 2010. This work entailed the design of low-power, high-speed, and wide interconnection methods with the goal of transmitting data to/from the memory module and the MC at higher speeds.

12. I have extensive experience in the development of instrumentation and commercial products in a multitude of areas including: integrated electrical/biological circuits and systems, array (memory, imagers, and displays) circuit design, CMOS analog and digital circuit design, diagnostic electrical and electro-optic instrumentation for scientific research, CAD tool development and online tutorials, low-power interconnect and packaging techniques, design of communication/interface circuits (to meet commercial standards such as USB, firewire, DDR, PCIe, SPI, etc.), circuit design for the use and storage of renewable energy, and power electronics. For example, a part of my research at Boise State, for many years, focused on the use of Thru-Silicon-Vias (TSVs), aka Thru-Wafer Vias (TWVs), for high-density 3D packaging. These packaging techniques were utilized in the memory module development work I did with Sun Microsystems and Oracle. As another example, I designed circuitry for use in implementing Universal Serial Bus (USB) interface circuits while I did consulting at Tower Semiconductor. I designed PCI communication circuits for IPC between a Graphics Processor Unit (GPU) and memory while consulting for Rendition, Inc. From 1994 to 1996, I worked on the design of displays at MTI. This work was at a time when cathode ray tubes (CRTs) were still the dominant type of display. Flat panel displays were being developed with the hope of replacing CRTs in the consumer market. I worked on flat panel displays which resulted in five patents: U.S. Patent Nos. 5,598,156, 5,638,085, 5,818,365, 5,894,293, and 5,909,201. I worked on the design of the pixels, both active and passive, as well as the supporting electronics for processing video signals. I was involved with the evaluation of display technologies including liquid crystal displays (LCDs), light-emitting diodes, plasma displays, and organic light emitting diode (OLED) displays; the display technologies that were looking to displace CRTs in the consumer market. I was also involved with the packaging of the displays including the vacuum sealing and deposition of the

phosphors for light wavelength conversion. I also taught display design as a topic in my courses and did display design consulting again in industry for Cirque in 2013.

13. My current research work is focused in part on the design of integrated circuits for wireless sensing using LIDAR (LIght Detection And Ranging). I have worked with several companies in the development of these circuits and systems including Freedom Photonics, Aerius Photonics, and FLIR. In the early 1990s, I worked on wireless systems for wideband impulse radar while at Lawrence Livermore Laboratory. Further, part of my research for several years focused on the digitization of IQ channels using delta-sigma modulation. The knowledge and experience gained from this effort are reflected in my textbook CMOS Mixed-Signal Circuit Design and a presentation, which I have presented at several universities and companies, http://cmosedu.com/jbaker/papers/talks/BP_DSM_talk.pdf.

C. Academic Experience

14. I was an adjunct faculty member in the Electrical Engineering departments of UNLV and UNR from 1991-1993. From 1993 to 2000, I served on the faculty at the University of Idaho as an Assistant Professor and then as a tenured Associate Professor of Electrical Engineering. In 2000, I joined a new Electrical and Computer Engineering program at Boise State University ("BSU"), where I served as department chair from 2004 to 2007. At BSU, I helped establish graduate programs in Electrical and Computer Engineering including, in 2006, the university's second Ph.D. degree. In 2012, I re-joined the faculty at UNLV. Over the course of my career as a professor, I have advised more than 100 masters and doctoral students.

15. I have been recognized for my contributions as an educator in the field. While at BSU, I received the President's Research and Scholarship Award (2005), Honored Faculty Member recognition (2003), and Outstanding Department of Electrical Engineering Faculty recognition (2001). In 2007, I received the Frederick Emmons Terman Award (the "Father of

Silicon Valley"). The Terman Award is bestowed annually upon an outstanding young electrical/computer engineering educator in recognition of the educator's contributions to the profession. In 2011, I received the IEEE Circuits and Systems Education Award. I received the Tau Beta Pi Outstanding Electrical and Computer Engineering Professor Award every year it was awarded while I have been back at UNLV.

16. I have authored several books and papers in the electrical and computer engineering area. My published books include CMOS Circuit Design, Layout, and Simulation (Baker, R.J., Wiley-IEEE, ISBN: 9781119481515 (4th ed., 2019)) and CMOS Mixed-Signal Circuit Design (Baker, R.J., Wiley-IEEE, ISBN: 9780470290262 (2nd ed., 2009) and ISBN: 9780471227540 (1st ed., 2002)). I co-authored DRAM Circuit Design: Fundamental and High-Speed Topics (Keeth, B., Baker, R.J., Johnson, B., and Lin, F., Wiley-IEEE, ISBN: 9780470184752 (2008)), DRAM Circuit Design: A Tutorial (Keeth, B. and Baker, R.J., Wiley-IEEE, ISBN: 0-7803-6014-1 (2001)), and CMOS Circuit Design, Layout and Simulation (Baker, R.J., Li, H.W., and Boyce, D.E., Wiley - IEEE, ISBN: 9780780334168 (1998)). I contributed as an editor and co-author on several other electrical and computer engineering books.

D. Other Relevant Experience

17. I have performed technical and expert witness consulting for more than 200 companies and their subsidiaries and given more than 50 invited talks at conferences, companies, and universities. Further, I am the author or co-author of more than 100 papers and presentations in the areas of electrical and computer engineering design, fabrication, and packaging.

18. I currently serve, or have served, as a volunteer on the IEEE Press Editorial Board (1999-2004); as editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-2018); as the Technical Program Chair of the 2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS 2015); on the IEEE Solid-State Circuits Society (SSCS)

Administrative Committee (2011-2016); as a Distinguished Lecturer for the SSCS (2012-2015); the Technology Editor (2012-2014) and Editor-in-Chief (2015-2020) for IEEE Solid-State Circuits Magazine; IEEE Kirchhoff Award Committee (2020-2023); and advisor for the student branch of the IEEE at UNLV (2013-present). These meetings, groups, and publications are intended to allow researchers to share and coordinate research. My active participation in these meetings, groups, and publications allowed me to see what other researchers in the field have been doing.

19. In addition to the above, I am an IEEE Fellow for contributions to semiconductor memory design and a member of the honor societies Eta Kappa Nu and Tau Beta Pi.

II. SUMMARY OF THE ’339 PATENT

A. Overview of the ’339 Patent

20. The ’339 Patent purports to teach techniques for handling communication between processor cores of a multi-core processor. ’339 Patent at Abstract. The objective of the ’339 Patent is provided below:

> ***Embodiments of the disclosure generally set forth techniques for handling communication between processor cores.*** Some example multi-core processors include a first set of processor cores in a first region of the multi-core processor configured to dynamically receive a first supply voltage and a first clock signal, a second set of processor cores in a second region of the multi-core processor configured to dynamically receive a second supply voltage and a second clock signal, and an interface block coupled to the first set of processor cores and the second set of processor cores, wherein the interface block is configured to facilitate communications between the first set of processor cores and the second set of processor cores.

Id. at Abstract.

21. Figure 1 shows four sets of processor cores with the first set highlighted in green and the second set highlighted in red.

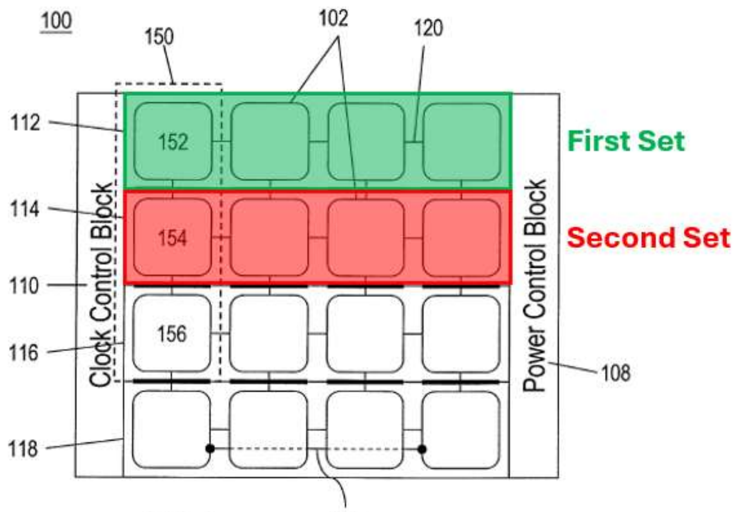


FIG. 1

22. Figures 2 and 3 show an interface block (highlighted in blue) coupled to the first set of processor cores (again highlighted in green) and also coupled to the second set of processor cores (again highlighted in red):

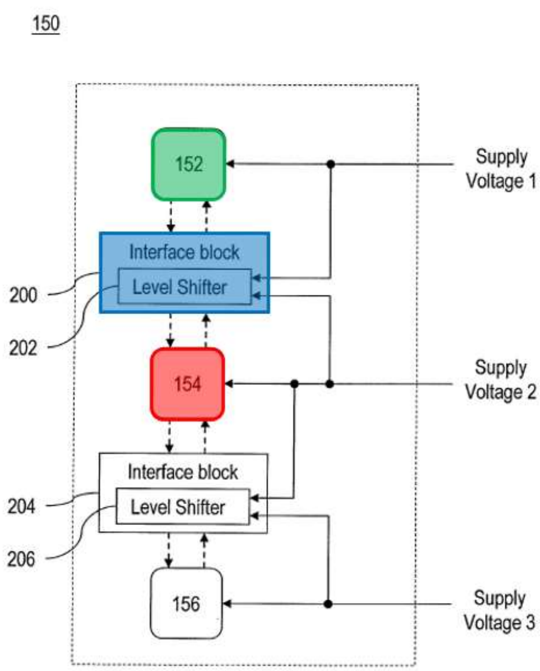


FIG. 2

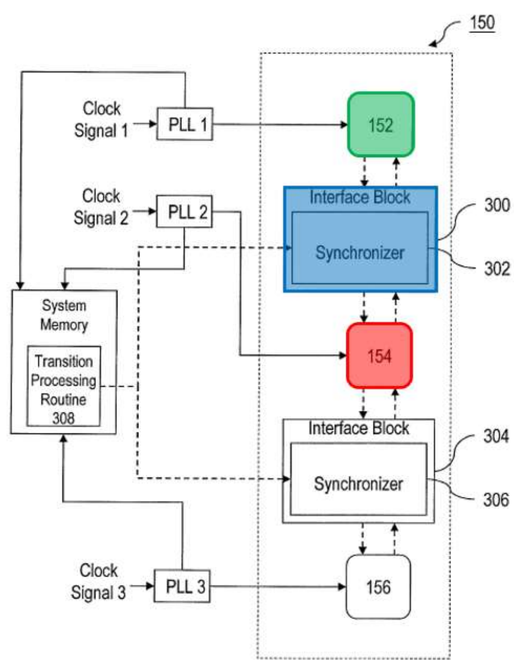


FIG. 3

23. The '339 Patent discloses that for power consumption management, independent voltage supply and clock speed control is utilized for the first set and the second set of processor cores, such that the multi-core processor may operate at high power and high clock frequency when needed and at low power when the computing requirements are reduced. *Id.* at 1:10-14. In this regard, the object of the '339 Patent is as follows:

> A multi-core processor includes two or more independent processor cores arranged in an array. Each processor core in a conventional multi-core processor generally shares the same supply voltage and clock signal to simplify the interfaces between the processor cores. ***For power consumption management, dynamic supply voltage and clock speed control may be utilized, so that a multi-core processor may operate at high power and high clock frequency when needed and at low power when the computing requirements are reduced.***

Id. at 1:6-14.

24. The power profiles for the first set and the second set of processor cores are independent of each other. Similarly, the clock signals of the first set and the second set of processor cores are independent of each other. *Id.* at 2:25-31. Further elaboration is provided below:

> For example, the multi-core processor 100 may be divided into stripes 112, 114, 116, and 118. ***Each stripe may be associated with an independent power profile. For example, the stripe 112 may be powered by a supply voltage received from a power control block 108 and/or may be associated with an independent clock domain defined by a clock signal received from a clock control block 110.***

Id. at 2:25-31.

> ***The power profile associated with a stripe may be determined based on the computational requirements of the tasks assigned to the processor cores in the stripe***.

Id. at 2:41-43.

25. As such, facilitating communication between two processor cores is necessary and is performed by interface blocks. *Id.* at 3:21-23. Further disclosures of interface blocks, such as having a level shifter or a synchronizer, are provided below:

> ***The processor core 152 may be powered by a supply voltage 1 and coupled to an interface block 200 having a level shifter 202***; the processor core 154 may be powered by a supply voltage 2 and coupled to the same interface block 200; and ***the processor core 156 may be powered by a supply voltage 3 and coupled to an interface block 204 having a level shifter 206.***

Id. at 3:30-36.

> ***The processor core 152 may be driven by a clock signal 1 and coupled to an interface block 300 having a synchronizer 302***; the processor core 154 may be driven by a clock signal 2 and coupled to the same interface block 300; and ***the processor core 156 may be driven by a clock signal 3 and coupled to an interface block 304 having a synchronizer 306***.

Id. at 4:4-10.

B. Priority Date for the ’339 Patent

26. I have reviewed the prosecution history of the ’339 Patent. The ’339 Patent issued from U.S. Patent Appl. No. 12/713,220 (the "’220 Application") and does not purport to claim domestic priority or foreign priority to any other application. The earliest possible priority for the ’339 Patent is therefore February 26, 2010. I have been asked to assume this earliest date as the priority date.

III. LEGAL BASES OF OPINIONS

A. Level of Ordinary Skill in the Art

27. I have been informed that both the ’339 Patent is to be understood from the perspective of a hypothetical person having ordinary skill in the art at the time of the purported inventions claimed in the ’339 Patent (a "PHOSITA"). I have been asked to treat the earliest possible priority date of February 26, 2010, as the time of the purported inventions claimed in the ’339 Patent for purposes of this proceeding.

28. I understand that the factors that may be considered to determine the level of ordinary skill in the art include: (a) the type of problems encountered in the art; (b) prior art solutions to those problems; (c) the complexity or sophistication of the technology in the art; (d)

the education level and experience of active workers in the field of art; and (e) the pace of change, development, and innovation in the field of art. I have been informed that not every factor would be present in every case, and that a review of the prior art would shed light on factors (a), (b), (c), and (e). I have also been informed that a PHOSITA is further presumed to have been aware of all relevant prior art.

29. The ’339 Patent is directed to communication between processor cores of a multi-core processor. The claims incorporate common elements including a multi-core processor, supply voltages, clock signals, and interface blocks. I am familiar with the state of the art in this field at the time of the purported inventions claimed in the ’339 Patent.

30. In my opinion, a PHOSITA would have had a minimum of a bachelor’s degree in electrical engineering, computer engineering, computer science, or a similar field, and at least two years of industry or academic experience designing or analyzing electronic circuits, semiconductors, processors, or power management, and related firmware and software, or the equivalent. The more education one has (e.g., additional studies, coursework, or degrees), the less experience needed to attain an ordinary level of skill. Likewise, more extensive experience might substitute for some educational requirements.

31. In view of my educational background and my decades of academic and professional experience (as discussed above), I was a person of more than the ordinary level of skill in the art in the early 2010 timeframe. My opinions expressed in this declaration were formed, however, from the perspective of a person of ordinary skill in the art as of February 26, 2010. I was, and am, well acquainted with the level of knowledge of a PHOSITA under this definition. As noted above, I have worked with many individuals during my time in the industry and taught many who would have met the definition of a PHOSITA. Thus, I am comfortable applying this viewpoint

in assessing the ’339 Patent and the state of the art in the relevant timeframe.

32. I have also considered whether my opinions expressed in this declaration would change if the level of ordinary skill in the art was varied by some minor amount of time or varied somewhat with respect to subject matter. My opinions would not change in light of such minor variations.

B. Claim Construction

33. I have been informed that patent claims are to be interpreted from the perspective of PHOSITA. I have also been informed that the words of a patent claim are generally given their ordinary and customary meaning to a PHOSITA in view of the context of the claims and the intrinsic evidence, *i.e.*, the patent specification and the prosecution history of the ’339 Patent. I have read and analyzed the claims of the ’339 Patent from this perspective.

34. I have been further informed that extrinsic evidence, *e.g.*, prior art publications and expert testimony, may be considered to understand a patent claim, but cannot be used to contradict an interpretation thereof which is unambiguous in view of the intrinsic evidence.

35. I understand that claims must particularly point out and distinctly claim the invention in the patent. I understand that a claim is deemed indefinite if it fails to inform those skilled in the art about the scope of the invention with reasonable certainty when interpreted in light of the specification and the prosecution history.

IV. ASSERTED CLAIMS OF THE ’339 PATENT

36. I understand that Claims 1, 5, 8-10, 14, and 21 are asserted in this litigation. These claims are reproduced below:

1[pre]	A multi-core processor, comprising:
1[a1]	a first set of processor cores of the multi-core processor,

1[a2]	wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage and a first output clock signal of a first phase lock loop (PLL) having a first clock signal as input;
1[b1]	a second set of processor cores of the multi-core processor,
1[b2]	wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage and a second output clock signal of a second PLL having a second clock signal as input,
1[b3]	wherein the first supply voltage is independent from the second supply voltage, and
1[b4]	the first clock signal is independent from the second clock signal; and
1[c1]	an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores,
1[c2]	wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores.
5[pre]	The multi-core processor of claim 1,
5[a]	wherein the first set of processor cores and the second set of processor cores are configured to receive one or more control signals from one or more control blocks located in a periphery of the multi-core processor.
8[pre]	The multi-core processor of claim 1,
8[a]	wherein the first set of processor cores are located in a first region of the multi-core processor, and the second set of processor cores are located in a second region of the multi-core processor.
9[pre]	The multi-core processor of claim 8,
9[a]	wherein the first region and the second region are overlapping regions of the multi-core processor.
10[pre]	The multi-core processor of claim 8,
10[a]	wherein the first region and the second region are non-overlapping regions of the multi-core processor.
14[pre]	The multi-core processor of claim 1,
14[a]	wherein the first set of processor cores and the second set of processor cores are configured to receive one or more control signals from one or more control blocks located in a common region that is substantially central to the first set of processor cores and the second set of processor cores.
21[pre]	A multi-core processor, comprising:
21[a1]	a first set of processor cores of the multi-core processor,
21[a2]	wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage from a power control block and a first output clock signal from a first phase lock loop (PLL) having a first clock signal as input in a clock control block;
21[b1]	a second set of processor cores of the multi-core processor,
21[b2]	wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage from the power control block and a second output clock signal from a second PLL having a second clock signal as input in the clock control block,
21[b3]	wherein the first supply voltage is independent from the second supply voltage, and

21[b4]	the first clock signal is independent from the second clock signal; and
21[c1]	an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores,
21[c2]	wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores.

V. DISPUTED TERMS

A. "each processor core from the first/second set of processor cores is *configured to dynamically receive* a first/second supply voltage [from a power control block] and a first/second output clock signal" (Claims 1, 21)

37. A PHOSITA would not be able to determine with reasonable certainty the scope of the term "configured to dynamically receive" within the contested claim phrase, "each processor core from the first/second set of processor cores is configured to dynamically receive a first/second supply voltage [from a power control block] and a first/second output clock signal." For instance, a PHOSITA would not understand what distinguishes processor cores that are configured to dynamically receive a supply voltage or clock signal from cores that are configured to receive such signals statically or not dynamically.

38. A PHOSITA would not readily ascertain the scope of this claim phrase based on the claims, specification, and file history of the '339 Patent. After all, "configured to dynamically receive," does not have an understood meaning in this field, and the lack of any context in the '339 Patent exacerbates this problem.

39. In fact, the phrase "configured to dynamically receive" does not appear anywhere in the intrinsic evidence except in the claims of the '339 Patent, including asserted Claims 1 and 21, as I outlined above. However, the '339 Patent does disclose processor cores that are simply "configured to receive" signals, which is a common function of processor cores. For example, Claims 5 and 14 recite, "wherein the first set of processor cores and the second set of processor cores ***are configured to receive*** one or more control signals from one or more control blocks." The '339 Patent does not explain how a processor core "configured to ***dynamically*** receive" voltage

and clock signals, as recited in Claims 1 and 21, is different from receiving voltage and clock signals non-dynamically.

40. While a PHOSITA would understand that the term "dynamic" conveys something that is changing as opposed to something that remains the same or "static," a PHOSITA would not know whether "dynamically" refers to changes (e.g., in time, voltage levels, frequencies, etc.) above a specific threshold or even what that threshold might be. Likewise, a PHOSITA would understand that voltage and clock frequencies can be adjusted in response to processing or power consumption needs, a PHOSITA would not know whether the modifier, "dynamically," connotes a specific threshold rate at which those changes occur and/or a specific threshold regarding the degree of those changes.

41. Furthermore, the '339 Patent discusses "dynamic" supply and clock speed control and "dynamically" adjusting power profiles ('339 Patent at 1:10-14, 2:26-31, 2:41-60, 3:17-30), but it does not describe how processor cores are "configured to dynamically receive" signals, which is a separate issue. Critically, a PHOSITA is left in the dark after reading the intrinsic evidence regarding what the metes and bounds of that functionality is and what objective standards could be used to determine whether a particular processor cores was "dynamically" receiving signals, given the varying changes and fluctuations that could be involved, as I discussed above.

42. Accordingly, it is my opinion that "configured to dynamically receive" in the disputed, larger phrases in Claims 1 and 21 would not apprise a PHOSITA of the scope of the claims with reasonable certainty.

43. For the foregoing reasons, it is my opinion that the term is indefinite.

B. "one or more control blocks located in a periphery of the multi-core processor" (Claim 5)

44. Claim 5 of the '339 Patent recites that the first set of processor cores and second

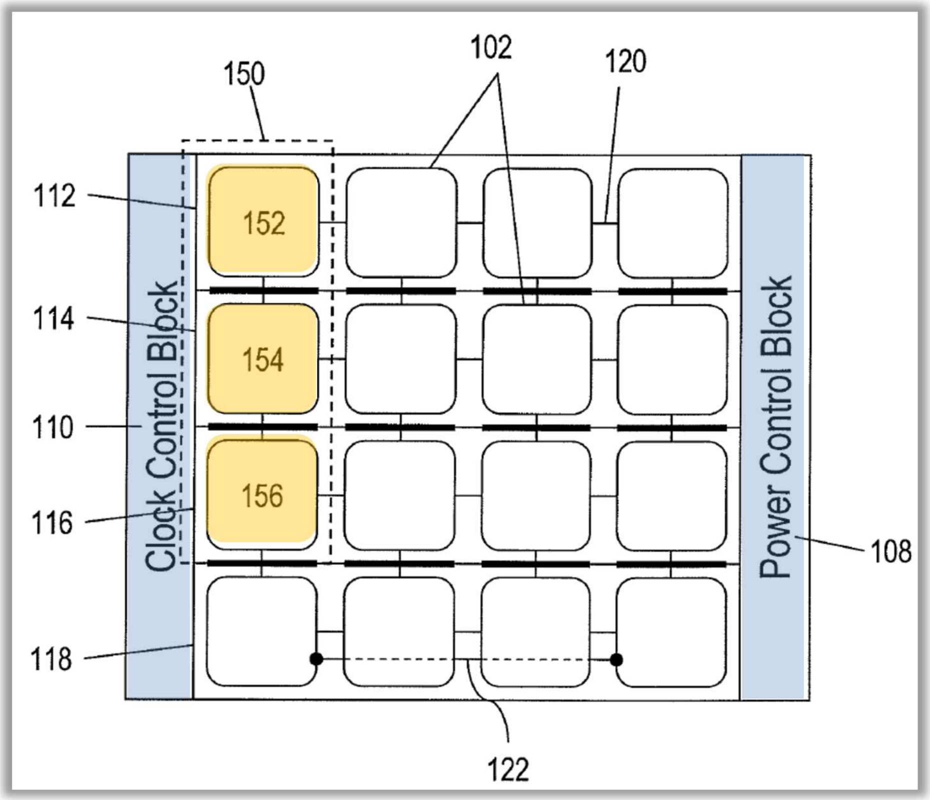
set of processor cores of the "multi-core processor of claim 1" are "configured to receive one or more control signals from one or more control blocks located in a ***periphery*** of the multi-core processor." '339 Patent, Claim 5. However, the undefined term of degree, "periphery," only appears in one place in the specification: "A power profile associated with an individual processor core may be controlled through signals that may be received from control blocks that are located in the periphery of the multi-core processor." '339 Patent at 1:61-65. Therefore, in the only place where this term is discussed, no guidance is provided on how to measure the bounds of what constitutes the "periphery" of the processor with any degree of certainty.

45. This problem is compounded by the apparent contrasting of locations in other parts of the specification. In particular, the '339 Patent discloses that "the power control block 108 and the clock control block 110 may be arranged at two different sides of the multicore processor 100" or "at the same side," which is contrasted with other implementations where "the power control block 108 and the clock control block 110 may be arranged in a common area located near the center of the multi-core processor 100":

> The multi-core processor 100 may be further divided into regions. In some implementations, the regions of multi-core processor 100 may correspond to rows of the two-dimensional array, and the regions may or may not be overlapping. Each row of processors may also be referred to as a "stripe." For example, the multi-core processor 100 may be divided into stripes 112, 114, 116, and 118. Each stripe may be associated with an independent power profile. For example, the stripe 112 may be powered by a supply voltage received from a power control block 108 and/or may be associated with an independent clock domain defined by a clock signal received from a clock control block 110. In some implementations, the power control block 108 and the clock control block 110 may be arranged at two different sides of the multicore processor 100 as shown in FIG. 1. In some other implementations, the power control block 108 and the clock control block 110 may be arranged at the same side of the multi-core processor 100. In yet some other implementations, the power control block 108 and the clock control block 110 may be arranged in a common area located near the center of the multi-core processor 100.

'339 Patent at 2:20-40.

46. As seen above, this part of the specification does not discuss where the periphery is located or the bounds of that apparent region of the processor, but it states that an arrangement of control blocks on "two different sides of the multicore processor" are "shown in FIG. 1." Figure 1 (below, with **blue** highlighting around the control blocks and **orange** highlighting around the processor cores), shows those blocks at the very edge of the processor core:



47. There is no indication that this necessarily corresponds to the "periphery" of the processor, or how to draw the box of what constitutes the "edge" or "periphery. This confusion is amplified by other figures in the '339 Patent. For instance, Figure 3 shows the same cores 152, 154, and 156 from Figure 1. But, again, there is no indication of where the control blocks would be, whether at the periphery or centrally located or some other configuration. This is represented in Figure 3 below, in which it is unclear where the periphery is located for housing the control

blocks, as it could be any undefined space around the processor cores (an undefined region highlighted in **blue** for possible control block locations is shown below, in which the undefined region could extend into what could be considered both central and peripheral locations according to conflicting disclosures in the '339 Patent). This shows that the location is an arbitrary and subjective determination without objective guidance in the '339 Patent.

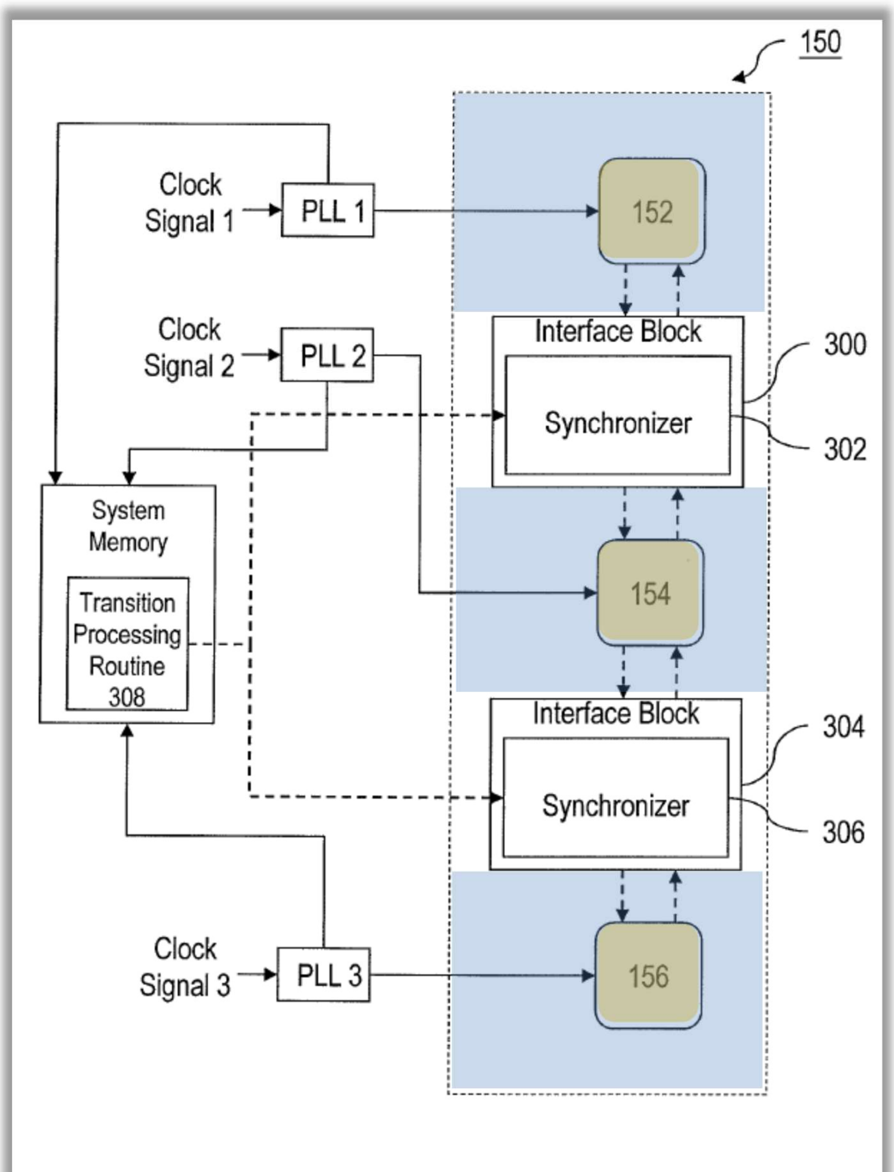


FIG. 3

48. The ’339 Patent also does not provide any functional guidance on this term. In other words, the ’339 Patent provides no discussion or indication that the location of the control blocks, whether periphery, centrally or otherwise located relative to the multi-core processor, would in any way limit or alter their function in providing control signals. There is no explanation as to how the positioning would affect their functionality. A PHOSITA would have understood that the placement of control blocks does not affect the function of providing control signals for managing or coordinating the operations of processor cores. Instead, a PHOSITA would have understood that this function depends on the logical connections and signal routing, rather than the physical location of the control block relative to the processor. Accordingly, the ’339 Patent also fails to provide reasonable clarity regarding the scope of “located in a periphery” even when a PHOSITA attempts to consider the functional impacts and disclosures (or, lack thereof) regarding that term.

49. Furthermore, while a PHOSITA understands what a “multi-core processor” is, the PHOSITA would also know that it might refer to multiple components or arrangements. For example, a PHOSITA could refer to multiple individual processor cores (e.g., processor cores 152, 154, and 156 in Figure 1, above) as a multi-core processor. In other situations, a PHOSITA may consider the complete die, containing the processor cores and additional circuitry, to be a “multi-core processor.” A PHOSITA could also refer to the packaged die as a “multi-core processor.” As such, it is unclear whether “periphery of the multi-core processor” might be limited to regions inside the multi-core processor within some unspecified distance of the boundary of the multi-core processor, however that boundary might be defined, or whether “periphery of the multi-core processor” also includes components outside the multi-core processor but within some unspecified distance of its boundary.

50. In other words, there is not a common understanding in this field regarding what constitutes the "periphery" of a "multi-core processor."

51. Accordingly, it is my opinion that "located in a ***periphery*** of the multi-core processor" in the disputed, larger phrase in Claim 5 would not apprise a PHOSITA of the scope of the claim with reasonable certainty.

52. For the foregoing reasons, it is my opinion that the term is indefinite.

C. "common region that is substantially central to the first set of processor cores and the second set of processor cores" (Claim 14)

53. This phrase suffers from some of the same ambiguity as the "peripheral" term, above.

54. This disputed phrase is part of the larger limitation of Claim 14 of the '339 Patent, which recites "wherein the first set of processor cores and the second set of processor cores are configured to receive one or more control signals from one or more control blocks located in a common region that is substantially central to the first set of processor cores and the second set of processor cores."

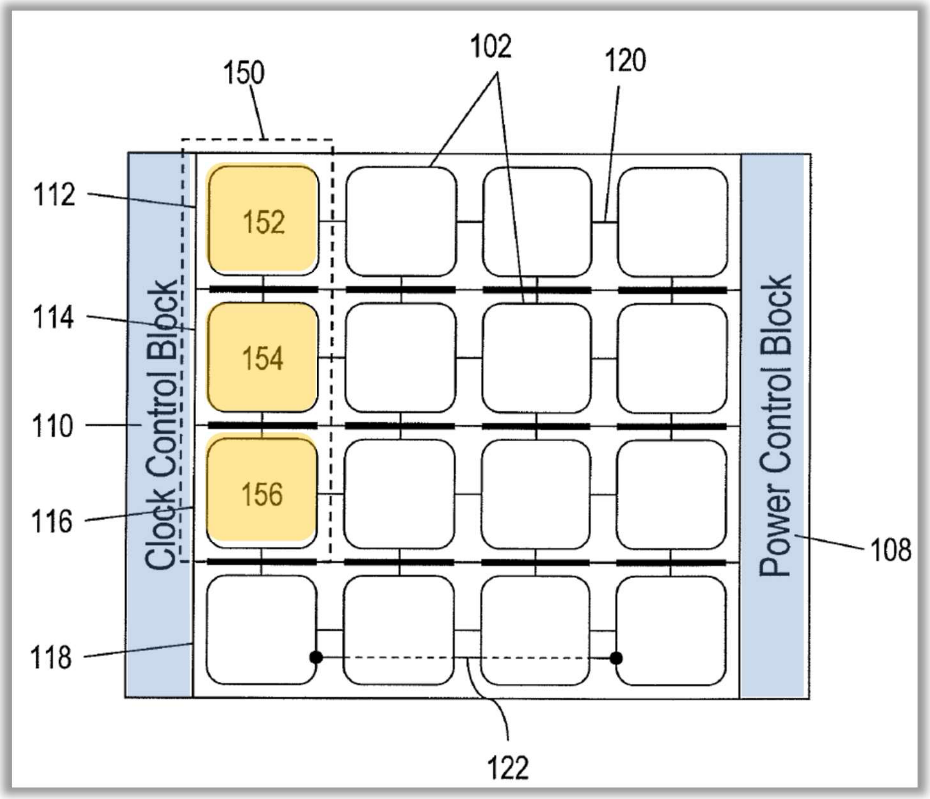
55. The intrinsic evidence does not inform a PHOSITA of the scope of this phrase with reasonable certainty. This problem is compounded by the apparent contrasting of locations in the specification. In particular, the '339 Patent discloses that "the power control block 108 and the clock control block 110 may be arranged at two different sides of the multicore processor 100" or "at the same side," which is contrasted with other implementations where "the power control block 108 and the clock control block 110 may be arranged in a common area located near the center of the multi-core processor 100":

> The multi-core processor 100 may be further divided into regions. In some implementations, the regions of multi-core processor 100 may correspond to rows of the two-dimensional array, and the regions may or may not be overlapping. Each row of processors may also be referred to as a "stripe." For example, the multi-core processor 100 may be divided into stripes 112, 114, 116, and 118. Each stripe may

> be associated with an independent power profile. For example, the stripe 112 may be powered by a supply voltage received from a power control block 108 and/or may be associated with an independent clock domain defined by a clock signal received from a clock control block 110. In some implementations, the power control block 108 and the clock control block 110 may be arranged at two different sides of the multicore processor 100 as shown in FIG. 1. In some other implementations, the power control block 108 and the clock control block 110 may be arranged at the same side of the multi-core processor 100. In yet some other implementations, the power control block 108 and the clock control block 110 may be arranged in a common area located near the center of the multi-core processor 100.

’339 Patent at 2:20-40.

56. As seen above, this part of the specification does not discuss where the disclosed regions are of the processor or their bounds. Again, an arrangement of control blocks on “two different sides of the multicore processor” are “shown in FIG. 1.” Figure 1 (below, with **blue** highlighting around the control blocks and **orange** highlighting around the processor cores), shows those blocks at the very edge of the processor core:



57. There is no indication that this shows a "common area" or one that is "substantially central" to two sets of processor cores. This confusion is amplified by other figures in the '339 Patent. For instance, Figure 3 shows the same cores 152, 154, and 156 from Figure 1. But, again, there is no indication of where the control blocks would be, whether at the periphery or centrally located or some other configuration. This is represented in Figure 3 below, in which it is unclear where the "common area is located or whether that area is "substantially central" to the cores, or what that box is defined to be (an undefined region highlighted in **blue** for possible control block locations is shown below, in which the undefined region could extend into what could be considered both central and peripheral locations according to conflicting disclosures in the '339 Patent). This shows that the location is an arbitrary and subjective determination without objective guidance in the '339 Patent.

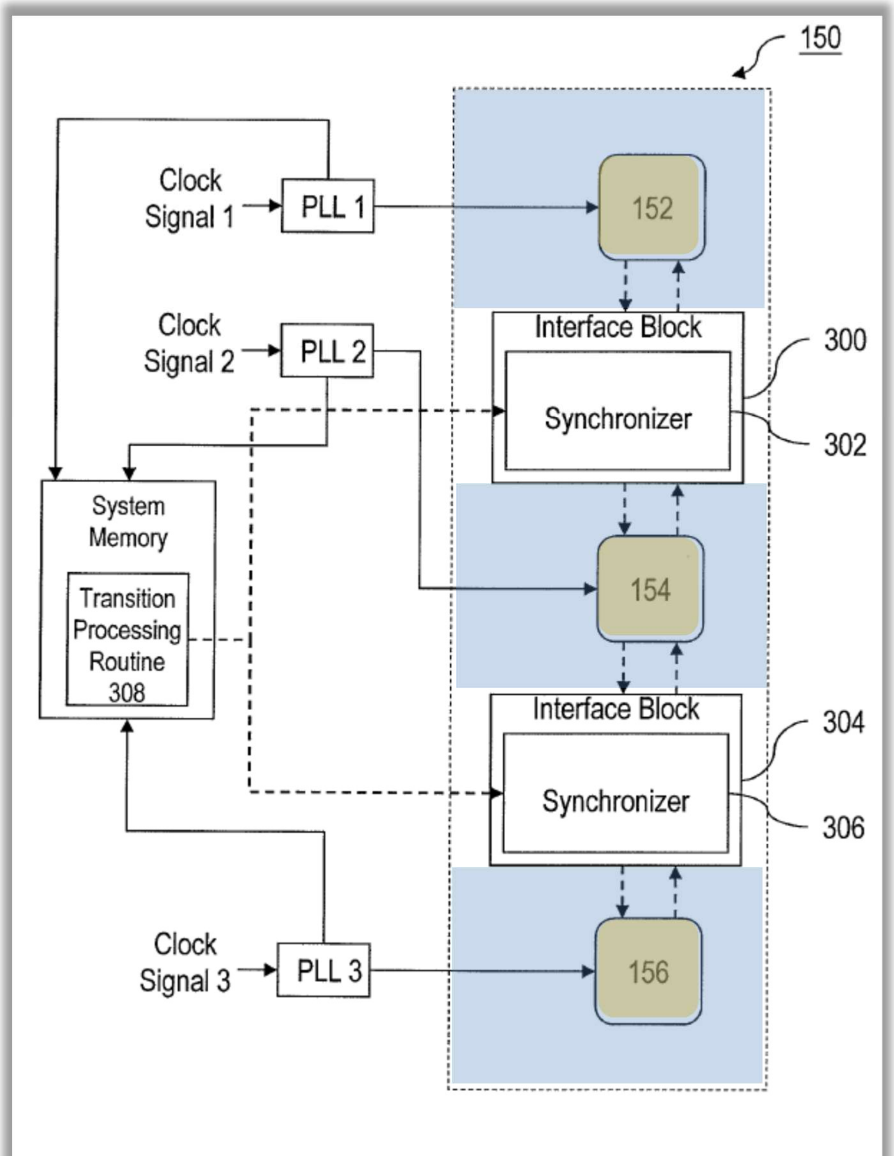


FIG. 3

58. The ’339 Patent also does not provide any functional guidance on this term. In other words, the ’339 Patent provides no discussion or indication that the location of the control blocks, whether periphery, centrally or otherwise located relative to the multi-core processor, would in any way limit or alter their function in providing control signals. There is no explanation as to how the positioning would affect their functionality. A PHOSITA would have understood

that the placement of control blocks does not affect the function of providing control signals for managing or coordinating the operations of processor cores. Instead, a PHOSITA would have understood that this function depends on the logical connections and signal routing, rather than the physical location of the control block relative to the processor. Accordingly, the ’339 Patent also fails to provide reasonable clarity regarding the scope of a “common region that is substantially central” even when a PHOSITA attempts to consider the functional impacts and disclosures (or, lack thereof) regarding that phrase.

59. In addition, neither “located in a common region” nor “substantially central” have a common understanding in this field such that a POSITA could determine with reasonably certainty what constitutes components “located in a common region” or whether such components are “substantially central” to the first and second sets of processor cores.

60. And the claim language does not shed any light regarding what constitutes a common region. While Claim 14 references a “common region,” other claim language creates ambiguity regarding what that means. Claim 8, for instance, which like Claim 14 depends directly from Claim 1, recites that the processor cores as located in a “region.” Specifically, Claim 8 states “the first set of processor cores are located in a first region of the multi-core processor, and the second set of processor cores are located in a second region of the multi-core processor.” A PHOSITA would not understand with reasonable certainty what delineates a region or what it means for such a “region” to be “common” between the first and second sets of processor cores. One reasonable interpretation of “common” would be “overlapping.” But “overlapping” regions are explicitly claimed in Claim 9, which depends from Claim 8 and states, in part, “wherein the first region and the second region are overlapping regions.” Thus, the ’339 Patent further injects confusion for a PHOSITA because while “common” could be interpreted to mean “overlapping,”

the ’339 Patent actually distinguishes “common” and “overlapping.” This confirms that a PHOSITA would not reasonably understand the metes and bounds of a “common region” in the context of the ’339 Patent.

61. Furthermore, the claims and the specification do not inform a PHOSITA as to the scope of the phrase “substantially central,” nor what it means for a “common region” to be “substantially central” to the first and second sets of processor cores. Indeed, the phrase “substantially central” is never used in the specification.

62. As discussed above for the “peripherally located” phrase, there are many different arrangements for multi-core processors. Without further guidance from the ’339 Patent, and there is none, a PHOSITA would not understand where “substantially central” is to be measured from and how to do so. For instance, in an arrangement where processor cores are in rows at various points on the die, such as at the top corners, it would be unclear whether “substantially central” would be in reference to the center of the die (i.e., in the center when measured from the vertical center line) or a reference to some middle point on the same horizontal center line as the two rows of processor cores. In other words, “substantially central” is a term of degree for a PHOSITA, and the ’339 Patent does not provide any objective criteria from which to measure that degree.

63. Accordingly, it is my opinion that disputed phrase, “common region that is substantially central to the first set of processor cores and the second set of processor cores,” would not apprise a PHOSITA of the scope of Claim 14 with reasonable certainty.

64. For the foregoing reasons, it is my opinion that the term is indefinite.

VI. RIGHT TO SUPPLEMENT

65. This declaration represents the opinions on the '339 Patent that I have formed to date. I reserve the right to revise, supplement, and/or amend my opinions stated herein based on new information that becomes available to me and on my continuing analysis of the materials already provided. In connection with any arguments raised by plaintiff, opinions by plaintiff's expert(s), additional evidence and testimony, and/or judicial determinations, whether in this or a related proceeding, I reserve the right to supplement my opinions in the future to respond thereto.

66. I declare under penalty of perjury under the laws of the United States that the foregoing is true and correct.

Dated: December 4, 2024, in Las Vegas, Nevada.

R. Jacob Baker, Ph.D., P.E.

APPENDIX A

R. JACOB BAKER, PH.D., P.E.

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PROFESSIONAL SUMMARY

Russel Jacob Baker (R. Jacob Baker), Ph.D., P.E. (IEEE Student Member 1983, Member 1988, Senior Member 1997, and Fellow 2013) was born in Ogden, Utah, on October 5, 1964. He received the B.S. and M.S. degrees in electrical engineering from the University of Nevada, Las Vegas (UNLV) in 1986 and 1988. He received the Ph.D. degree in electrical engineering from the University of Nevada, Reno (UNR) in 1993. His Google Scholar profile is here and his ResearchGate profile is here.

From 1981-1987 he served in the United States Marine Corps (from September of 1982 in the Reserves, Fox Company, 2nd Battalion, 23rd Marines, 4th Marine Division). From 1985-1993 he worked for E. G. & G. Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for underground nuclear weapons tests at the Nevada Test Site. During this time he designed, and oversaw the fabrication and the electrical/mechanical manufacture of, over 30 electronic and electro-optic instruments including high-speed cable and fiber-optic receiver/transmitters, PLLs, frame- and bit-syncs for high-speed imaging, data converters, streak-camera sweep circuits, Pockels cell drivers, micro-channel plate gating circuits, and analog oscilloscope electronics. From 1991-1993 he was an adjunct faculty member in the Departments of Electrical Engineering at UNLV and UNR. From 1993-2000 he served on the faculty in the Department of Electrical Engineering at the University of Idaho (UI), first as an untenured assistant professor and then from 1998 as a tenured associate professor. In 2000 he joined a new electrical and computer engineering (ECE) program at Boise State University (BSU) where he was promoted to professor in 2002. He then served as the ECE department chair from 2004-2007. At BSU he helped establish graduate programs in ECE including, in 2006, the university's second PhD degree. In 2012 he rejoined the faculty at UNLV as a tenured full professor of ECE. During his tenure at the UI, BSU, and UNLV he has been the major professor to more than 100 graduate students.

Dr. Baker has done consulting for over 200 companies. His research/development activities are in: photonics, circuit design for wireless and wired communications, analog-to-digital/digital-to-analog data conversion and transmission, optoelectronics (imagers, displays, LIDARs, APDs, SiPMs, and associated electronics), analog and digital integrated circuit design and fabrication, design of diagnostic electrical and electro-optic instrumentation for scientific research, integrated electrical/biological circuits and systems, array (memory, imagers, and displays) fabrication and design, design of digital processors for signal processing, CAD tool development and online tutorials, low-power interconnect and packaging (electrical and optical) techniques, design of wired/wireless communication and interface circuits, circuit design for the use and storage of renewable energy, power electronics and power supply design, and the delivery of online engineering education. As a result of this work, he is the named inventor on over 150 US patents and the author of over 100 publications.

He is a member of the honor societies Eta Kappa Nu and Tau Beta Pi, a licensed Professional Engineer, a popular lecturer that has delivered over 50 invited talks around the world, an IEEE Fellow, and the author of the books CMOS Circuit Design, Layout, and Simulation, CMOS Mixed-Signal Circuit Design, and a coauthor of DRAM Circuit Design: Fundamental and High-Speed Topics. He received the 2000 Best Paper Award from the IEEE Power Electronics Society,

the 2007 Frederick Emmons Terman Award, the 2011 IEEE Circuits and Systems Education Award, and the 2021 Wiley-IEEE Press Textbook Award for the 4th Edition of his book CMOS Circuit Design, Layout, and Simulation.

His service activities include the IEEE Press Editorial Board (1999-2004), editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-2018), the Technical Program Chair of the 2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS 2015), the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016), Distinguished Lecturer for the SSCS (2012-2015), Technology Editor (2012-2014) and Editor-in-Chief (2015-2020) for the IEEE Solid-State Circuits Magazine, IEEE Kirchhoff Award Committee (2020-2023), and advisor for the student branch of the IEEE at UNLV (2013-2024).

INDUSTRY EXPERIENCE

2008 - present: Expert witness in intellectual property disputes in electrical, electro-optic, and computer engineering matters for: 1) district court and ITC patent disputes, 2) inter partes reviews at the PTAB, and 3) arbitrations and mediations.

2013 - 2022: Worked with Freedom Photonics, Santa Barbara, CA, on the integration, fabrication and design, of optoelectronics with CMOS integrated circuits. Work includes the design of compact optical transceivers for range finding applications, high-efficiency integrated silicon avalanche photodetectors for quantum key receivers, Geiger mode SiGe receivers for long-range communications, cryptography, and the fabrication of near-infrared focal plane arrays. Packaging and testing of numerous chips fabricated in both CMOS and SiGe technologies using LEDs, ILDs, PIN, APDs, and ROICs.

2017 - 2019: Worked with Vorpal Research Systems, Las Vegas, NV on the design of integrated circuit electronics and optoelectronics for optical transceivers used in LIDARs/LADARs.

2016 - 2019: Worked with Attollo Engineering on the design of transient digitizers for the capture of high-speed signals for range finders using LEDs and lasers in compact optical transceivers.

2013 - 2018: Working with Mission Support and Test Services, LLC (MSTS, formerly National Security Technologies, LLC, [NSTec]) on the Design and Fabrication of Integrated electrical/photonic application specific integrated circuit (ASIC) design for use in the implementation of diagnostic instrumentation.

2013 - 2015: Consultant for OmniVision. Working on integrating CMOS image sensors (CIS) with memory for very high-speed consumer imager products. Design specialty DRAM, high-speed interfaces between CIS and DRAM, packaging techniques to pair the CIS with DRAM.

2010 - 2013: Worked with Arete' Associates on the design of high-speed compressive transimpedance amplifiers for LADAR projects and the design of ROIC unit cells. Work funded by the U. S. Air Force.

2013: Cirque, Inc. Consulting on the design of analog-to-digital interfaces for capacitive touch displays and pads.

2012: Consultant at Lockheed-Martin Santa Barbara Focal Plane Array. CMOS circuit design and fabrication for the development and manufacture of infrared components and imaging systems with an emphasis on highest sensitivity Indium Antimonide (InSb) focal plane arrays (FPAs) in linear through large staring formats. Product groups include FPAs, integrated dewar assemblies (IDCAs), camera heads, high-speed interfaces between image processors and imaging systems, and infrared imaging systems.

2010 - 2012: Working with Aerius Photonics (and then FLIR Inc. when Aerius was purchase by FLIR) on the design of Focal Plane Arrays funded (SBIRs and STTRs) by the U.S. Air Force, Navy, and Army. Experience with readout integrated circuits (ROICs) and the design/layout of photodetectors in standard CMOS.

2009 - 2010: Sun Microsystems, Inc. (and then Oracle) VLSI research group. Provided consulting on memory circuit design/fabrication and proximity connection (PxC) interfaces to DRAMs and SRAMs for lower power, 3D packaging, for memory modules and controllers implemented with FPGAs and custom ASICs.

2009 - 2010: Contour Semiconductor, Inc. Design of NMOS voltage and current references as well as the design of a charge pump for an NMOS memory chip.

1994 - 2008: Affiliate faculty (Senior Designer), Micron Technology. Designed CMOS circuits for DRAMs including DLLs, PLLs for embedded processors, voltage references and regulators, data converters, field-emitting display drivers, sensing for MRAM (using delta-sigma data conversion topologies), SRAMs, RFIDs, CMOS active pixel imagers and sensors, power supply design (linear and switching), input buffers, etc. Worked on a joint research project

between Micron and HP labs in magnetic memory fabrication and design using the MTJ memory cell. Worked on numerous technologies ranging from LED lighting to medical imaging using CMOS image sensors (too many to list) resulting in numerous US patents (see following list). Considerable experience working with product engineering to ensure high-yield from the production line from fabrication to test. Co-authored a book on DRAM circuit design through the support of Micron. Gained knowledge in the entire memory design process from fabrication to packaging. Developed, designed, and tested circuit design techniques for multi-level cell (MLC) Flash memory using signal processing.

January 2008: Consultant for Nascentric located in Austin, TX. Provide directions on circuit operation (DRAM, memory, and mixed-signal) for fast SPICE circuit simulations.

May 1997 - May 1999: Consultant for Tower Semiconductor, Haifa, Israel. Designed CMOS integrated circuit cells for various modem chips, interfaces, and serial buses including USB circuits, charging circuits based upon power up/down circuits using an MOS or bandgap reference, pre-amplifiers, comparators, etc.

Summer 1998: Consultant for Amkor Wafer Fabrication Services, Micron Technology, and Rendition, Inc., Design PLLs and DLLs for custom ASICs and processors.

Summers 1994 - 1995: Micron Display Inc. Designing phase locked loop for generating a pixel clock for field emitting displays and a NTSC to RGB circuit on chip in NMOS. These displays are miniature color displays for camcorder and wrist watch size color television. Worked on the fabrication and design of video peripheral circuits for these displays.

September - October 1993: Lawrence Berkeley Laboratory. Designed and constructed a 40 A, 2 kV power MOSFET pulse generator with a 3 ns rise-time and 8 ns fall-time for driving Helmholtz coils.

Summer 1993: Lawrence Livermore National Laboratory, Nova Laser Program. Researched picosecond instrumentation, including time-domain design for impulse radar and imaging.

December 1985 - June 1993: (from July 1992 to June 1993 employed as a consultant while finishing up my Ph.D.), E.G.&G. Energy Measurements Inc., Nevada, Senior Electronics Design Engineer. Responsible for the design and manufacturing of instrumentation used in support of Lawrence Livermore National Laboratory's Nuclear Test Program. Responsible for designing and fabricating over 30 electronic and electro-optic instruments including: CCD camera design, communication networks, fiber optic transmitters employing high speed laser drive electronics, receivers employing envelop tracking for DC voltage restoration and regeneration of received information, receiver low noise amplifier design, frame synchronizers for re-assembling transmitted images, high-speed SRAM memory system design with battery back-up, calibration equipment design such as a tunnel diode pulse generator for testing compensation of oscilloscopes and DAC design for calibrating CCD readout electronics, power supply and battery charger designs, sweep circuits for streak cameras, Pockel's cell drive electronics, vertical amplifier design using HBTs for analog oscilloscopes used at the Nevada Test Site, and 10 kV ramp designs using a planar triode to name some of the designs.

This position provided considerable fundamental grounding in EE with a broad exposure ranging from the design of PC boards to, for example, the design of cable equalizers. Summarizing, gained experience in circuit design technologies including: bipolar, vacuum tubes (planar triodes for high voltages), hybrid integrated circuit fabrication and design, GaAs (high speed logic and HBTs), Mach-Zehnder interferometers, Pockels cells, krytrons, power MOSFETs, microwave techniques, power supplies, fiber optic transmitters/receivers, etc.

Summer 1985: Reynolds Electrical Engineering Company, Las Vegas, Nevada. Gained hands on experience in primary and secondary power system design, installation and trouble-shooting electric motors on mining equipment.

ACADEMIC EXPERIENCE

January 1991 – present: Professor of Electrical and Computer Engineering at the **University of Nevada, Las Vegas** from August 2012 to present. From January 2000 to July 2012 held various positions at **Boise State University** including: Professor (2003 – 2012), Department Chair (2004 - 2007), and tenured Associate Professor (2000 - 2003). From August 1993 to January 2000 was a tenured/tenure track faculty member at the **University of Idaho**: Assistant Professor (1993 - 1998) and then tenured Associate Professor (1998 - 2000). Lastly, from January 1991 to May 1993 held adjunct faculty positions in the departments of Electrical Engineering at the University of Nevada, Las Vegas and Reno. Additional details:

- Research is focused on analog and mixed-signal integrated circuit fabrication and design. Worked with multi-disciplinary teams (civil engineering, biology, materials science, etc.) on projects that have been funded by EPA, DARPA, NASA, Army, DMEA, Navy, and the AFRL.
- Current and past research and development interests are:
  - Design and packaging of electrical/optical systems (e.g., LiDARs/LADARs) using LEDs, semiconductor lasers, lens for focusing and directing light, integrated circuits, and associated control and communication systems/circuits.
  - Capacitive sensing techniques using delta-sigma modulation and interfacing to sensors
  - Design of high-voltage and energy switching circuits
  - Circuit design and fabrication for the control, use, and storage of renewable energy using thermoelectric generators
  - Design of electrical/biological/optical circuits and systems using electrowetting on dielectric for automating and controlling biological experiments
  - Design of readout integrated circuits (ROICs) for use with focal plane arrays (FPAs)
  - Heterogeneous integration of III-V photonic devices (e.g., FPAs and VCSELs) with CMOS
  - Methods (e.g., 3D packaging and capacitive interconnects) to reduce power consumption in semiconductor memories, memory modules, and digital systems using custom and non-custom (e.g., FPGAs) implementations
  - Analog and mixed-signal circuit fabrication and design for communication systems, synchronization, energy storage, data conversion, and interfaces
  - The design of writing and sensing circuitry for emerging nonvolatile memory technologies, focal planes, and displays (arrays) in nascent nanotechnologies (e.g., magnetic, chalcogenide)
  - Reconfigurable electronics design and fabrication using nascent memory technologies such as the memristor to implement FPGAs
  - Finding an electronic, that is, no mechanical component, replacement for the hard disk drive using nascent fabrication technologies
  - Power electronics circuit design for consumers and consumer electronics including power management and adaptive control to reduce power consumption
  - Design of bandpass delta-sigma modulators for IQ demodulation in wireless communication systems in OFDM, WiFi, 802.11, Bluetooth, 3G, 4G, etc.
  - University prototyping, fabricating, and packaging of integrated circuits
- Led, as chair, the department in graduate curriculum (MS and PhD), program development, and ABET accreditation visits.
- Worked with established and start-up companies to provide technical expertise and identify employment opportunities for students.
- Held various leadership and service positions including: ECE chair, graduate coordinator, college curriculum committee (chair), promotion and tenure committee, scholarly activities committee, faculty search committee, university level search committees, etc. Collaborate with College of Engineering faculty on joint research projects.
- Taught courses in circuits, analog IC design, digital VLSI design and fabrication, fiber optics, and mixed-signal integrated circuit design to both on- and, via the Internet, off-campus students. Research emphasis in integrated circuit design using nascent technologies.

EDUCATION

- Ph.D. in Electrical Engineering; December 1993; University of Nevada, Reno, GPA 4.0/4.0. Dissertation Title: *Applying power MOSFETs to the design of electronic and electro-optic instrumentation.*
- M.S. and B.S. in Electrical Engineering: May 1986 and May 1988; University of Nevada, Las Vegas. Thesis Title: *Three-dimensional simulation of a MOSFET including the effects of gate oxide charge*.

MEMBERSHIPS IN PROFESSIONAL AND SCHOLARLY ORGANIZATIONS

IEEE (student, 1983; member, 1988; senior member, 1997; Fellow, 2013)
Member of the honor societies Eta Kappa Nu and Tau Beta Pi
Licensed Professional Engineer

HONORS AND AWARDS

- Consolidated Students of the University of Nevada, Las Vegas (CSUN) Faculty Award, 2017
- Tau Beta Pi UNLV Outstanding Professor of the Year in 2013, 2014, 2015 and 2016
- UNLV ECE Department Distinguished Professor of the Year in 2015
- IEEE Fellow for contributions to the design of memory circuits - 2013
- Distinguished Lecturer for the IEEE Solid-State Circuits Society, 2012 - 2015
- IEEE Circuits and Systems (CAS) Education Award - 2011
- Twice elected to the Administrative Committee of the Solid-State Circuits Society, 2011 - 2016
- Frederick Emmons Terman Award from the American Society of Engineering Education - 2007
- President's Research and Scholarship Award, Boise State University - 2005
- Honored Faculty Member - Boise State University Top Ten Scholar/Alumni Association 2003
- Outstanding Department of Electrical Engineering faculty, Boise State 2001
- Recipient of the IEEE Power Electronics Society's Best Paper Award in 2000
- University of Idaho, Department of Electrical Engineering outstanding researcher award, 1998-99
- University of Idaho, College of Engineering Outstanding Young Faculty award, 1996-97

SERVICE

Reviewer for IEEE transactions on solid-state circuits, circuits and devices magazine, education, instrumentation, nanotechnology, VLSI, etc. Reviewer for several American Institute of Physics journals as well (Review of Scientific Instruments, Applied Physics letters, etc.) Board member of the IEEE press (reviewed dozens of books and book proposals). Reviewer for the National Institutes of Health. Technology editor and then Editor-in-Chief for the Solid-State Circuits Magazine.

Led the Department on ABET visits, curriculum and policy development, and new program development including the PhD in electrical and computer engineering. Provided significant University and College service in infrastructure development, Dean searches, VP searches, and growth of academic programs. Provided university/industry interactions including starting the ECE department's advisory board. Held positions as the ECE department Master's graduate coordinator and coordinator for the Sophomore Outcomes Assessment Test (SOAT).

Also currently serves, or has served, on the IEEE Press Editorial Board (1999-2004), as a member of the first Academic Committee of the State Key Laboratory of Analog and Mixed-Signal VLSI at the University of Macau, as editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-2018), on the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016), as an Advisory Professor to the School of Electronic and Information Engineering at Beijing Jiaotong University, as a Distinguished Lecturer for the SSCS (2012-2015), as the Technical Program Chair for the IEEE 58th 2015 International Midwest Symposium on Circuits and Systems, MWSCAS 2015, as advisor for the student branch of the IEEE at UNLV (2013-2023), and as the Technology Editor (2012-2014) and Editor-in-Chief (2015-2020) for the *IEEE Solid-State Circuits Magazine*, and IEEE Kirchhoff Award Committee (2020-2023).

ARMED FORCES

From 1981 to 1987 served in the United States Marine Corps (from September of 1982 in the Reserves, Fox Company, 2nd Battalion, 23rd Marines, 4th Marine Division), Honorable Discharge. Military Occupational Specialty (MOS) was Machine Gunner (MOS 0331)

TEXTBOOKS AUTHORED

Baker, R. J., "CMOS Circuit Design, Layout and Simulation, Fourth Edition" *Wiley-IEEE Press*, 1234 pages. ISBN 9781119481515 (2019) **Over 50,000 copies of this book in print.** (Third Edition published in 2010, Revised Second Edition published in 2008, and Second Edition Published in 2005)

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Keeth, B., Baker, R. J., Johnson, B., and Lin, F., “DRAM Circuit Design: Fundamental and High-Speed Topics”, *Wiley-IEEE*, 2008, 201 pages. ISBN: 9780470184752

Keeth, B. and Baker, R. J., “DRAM Circuit Design: A Tutorial”, *Wiley-IEEE*, 2001, 201 pages. ISBN 0780360141

Baker, R. J., Li, H.W., and Boyce, D.E. "CMOS Circuit Design, Layout and Simulation," *Wiley-IEEE*, 1998, 904 pages. ISBN 9780780334168

BOOKS, OTHER (edited, chapters, etc.)

Saxena, V. and Baker, R. J., “Analog and Digital VLSI,” chapter in the CRC Handbook on Industrial Electronics, edited by J. D. Irwin and B. D. Wilamowski, *CRC Press*, 2009 second edition.

Baker, R. J., “CMOS Analog Circuit Design,” (A self-study course with study guide, videos, and tests.) IEEE Education Activity Department, 2000. ISBN 0-7803-4822-2 (with textbook) and ISBN 0-7803-4823-0 (without textbook)

Baker, R. J., “CMOS Digital Circuit Design,” (A self-study course with study guide, videos, and tests.) *IEEE Education Activity Department*, 2000. ISBN 0-7803-4812-5 (with textbook) and ISBN 0-7803-4813-3 (without textbook)

Li, H.W., Baker, R. J., and Thelen, D., “CMOS Amplifier Design,” chapter 22 in the CRC VLSI Handbook, edited by Wai-kai Chen, *CRC Press*, 1999 (ISBN 0-8493-8593-8) and the second edition in 2007 (ISBN 978-0-8493-4199-1)

INVITED TALKS AND SEMINARS

Have given over 50 invited talks and seminars at the following locations: AMD (Fort Collins), AMI semiconductor, Arizona State University, Beijing Jiaotong University, Boise State University, Carleton University, Carnegie Mellon, Columbia University, Dublin City University (Ireland), E.G.&G. Energy Measurements, Foveon, the Franklin Institute, Georgia Tech, Gonzaga University, Hong Kong University of Science and Technology, ICSEng Keynote, ICySSS keynote, IEEE Computing and Communication Workshop (CCWC), IEEE Electron Devices Conference (NVMTS), IEEE Workshop on Microelectronics and Electron Devices (WMED), Indian Institute of Science (Bangalore, India), Instituto de Informatica (Brazil), Instituto Tecnológico y de Estudios Superiores de Monterrey (ITESM, Mexico), Iowa State University, Lawrence Livermore National Laboratory, Lehigh University, Lockheed-Martin, Micron Technology, Nascentric, National Semiconductor, Princeton University, Rendition, Saintgits College (Kerala, India), Southern Methodist University, Sun Microsystems, Stanford University, ST Microelectronics (Delhi, India), Temple University, Texas A&M University, Tower Semiconductor (Israel), University of Alabama (Tuscaloosa), University of Arkansas, University of Buenos Aires (Argentina), University of Houston, University of Idaho, University of Illinois (Urbana-Champaign), Université Laval (Québec City, Québec), University of Macau, University of Maryland, Université de Montréal (École Polytechnique de Montréal), Xilinx (Ireland), University of Nevada (Las Vegas), University of Nevada (Reno), University of Toronto, University of Utah, Utah State University, and Yonsei University (Seoul, South Korea).

RESEARCH FUNDING

In-kind, equipment, and other non-contract/grant funding [e.g., MOSIS support, money for travel for invited talks, etc.] not listed.

- Baker, R. J., (2023-2024) "Silicon Germanium (SiGe) Avalanche Photo Diode (APD) Chip," Department of Energy, Mission Support and Test Services (MSTS), LLC, $120,000
- Baker, R. Jacob, (2017-2023) "Tiled Silicon Photomultiplier Array Read-Out Integrated Circuit," NASA, $29,999 (Phase I), $225,238 (Phase II), and $79,697 (Phase IIE)
- Goldman, J., Menezes, J., and Baker, R. J., (2021-2022) "Monitored Compression Therapy: Using Smart Technology to Optimize the Treatment of Lower Extremity Swelling," UNLV Sports Research & Innovation Initiative. Proof of Concept Grant Program, $50,000
- Baker, R. Jacob, (2019-2021) "Dual-Mode, Extended Near-Infrared, Focal Plane Arrays Fabricated with CMOS Compatible GeSiSn Alloy Materials," DARPA, $149,998
- Baker, R. Jacob, (2018-2020) “Geiger Mode SiGe Receiver for Long-Range Optical Communications,” NASA, $99,996

- Baker, R. Jacob, (2019) "Improved Quantum Efficiency Photo-Detector," Navy, $29,999
- Baker, R. Jacob, (2018-2019) "Tiled Silicon Photomultiplier Array Read-Out Integrated Circuit – Phase I," NASA, $29,999
- Baker, R. Jacob, (2017-2019) "Quantum Cryptography Detector Chip," Defense MicroElectronics Activity (DMEA), $266,029
- Baker, R. Jacob, (2017-2019) "Advanced Printed Circuit Board Design Methods for Compact Optical Transceiver," U.S. Army/DOD, $299,605
- Baker, R. Jacob, (2016-2018) "High-Sensitivity Monolithic Silicon APD and ROIC," U.S. Air Force/DOD, $299,665

DOCTORAL STUDENT SUPERVSION

10. Sachin Namboodiri – A Multi-channel MCP-PMT based Readout Integrated Circuit for LiDAR Applications (2020)
9. Wenlan Wu – High-Speed Radhard Mega-Pixel CIS Camera for High-Energy Physics (2019)
8. Kostas Moutafis – A Highly-Sensitive Global-Shutter CMOS Image Sensor with On-Chip Memory for Hundreds of kilo-frames per second Scientific Experiments (2019)
7. Yiyan Li – Portable High Throughput Digital Microfluidics and On-Chip Bacteria Cultures (2016)
6. Yacouba Moumouni – Designing, Building, and Testing a Solar Thermoelectric Generation, STEG, for Energy Delivery to Remote Residential Areas in Developing Regions (2015)
5. Qawi IbnZayd Harvard – Low-Power, High-Bandwidth, and Ultra-Small Memory Module Design (2011)
4. Vishal Saxena – K-Delta-1-Sigma Modulators for Wideband Analog-to-Digital Conversion (2010)
3. Robert Russell Hay – Digitally-Tunable Surface Acoustic Wave Resonator (2009)
2. Xiangli Li (the first Boise State University College of Engineering PhD graduate) – MOSFET Modulated Dual Conversion Gain CMOS Image Sensors (2008)
1. Feng Lin, Research and Design of Low Jitter, Wide Locking-Range Phase-Locked and Delay-Locked Loops (2000)

MASTERS STUDENT SUPERVISION

91. Jazmine Boloor – Survey of how Irregular Pathways in the Electrical System of the Human Heart Link to Different Heart Arrhythmias (2023)
90. Abraham Lopez – An Avalanche-Transistor-Based Pulse Generator Design For Infrared Laser Applications (2023)
89. David Santiago – Development of an Automated GPIB System for Characterization of SiGe Avalanche Photodiodes (2023)
88. Minsung Cho – Studies of Forward Projection Algorithms and Implementation on PC and FPGA (2023)
87. Armani Alvarez – A Control Integrated Circuit for a Hysteretic Flyback Power Converter (2022)
86. Francisco Mata-carlos – A Wearable Electronic Monitoring Device for Low Pressure Garment Applications and Temperature Analysis for Prevention of Ulceration and Infection (2022)
85. Daniel Senda – Designs and Outcomes of Transcranial Magnetic Stimulation (TMS) and Repetitive Transcranial Magnetic Stimulation (rTMS) Circuits (2021)
84. James Skelly – Monitored Compression Therapy: Using Smart Technology to Optimize the Treatment of Lower Extremity Swelling (2021)
83. Gonzalo Arteaga – Current-mode photon-counting circuit with SiGe BiCMOS input stage (2020)
82. Jason Silic – Design and Fabrication of a 6-bit Current-Mode ADC for Lidar and High-Speed Applications (2020)
81. Brandon Wade (2020)
80. Mario Valles Montenegro – Front-End CMOS Transimpedance Amplifiers on a Silicon Photomultiplier Resistant to Fast Neutron Fluence (2020)
79. Jonathan DeBoy (2018)
78. Dane Gentry – Design, Layout, and Testing of SiGe APDs Fabricated in a BiCMOS Process (2018)
77. James Mellot – Variable Transition Time Inverters in a Digital Delay Line with Analog Storage for Processing Fast Signals and Pulses (2018)
76. Eric Monahan – High Speed Fast Transient Digitizer Design and Simulation (2018)
75. Shada Sharif – Design and Analysis of First and Second Order K-Delta-1-Sigma Modulators in Multiple Fabrication Processes (2018)
74. Vikas Vinayaka – Analysis and Design of Analog Front-End Circuitry for Avalanche Photodiodes (APD) and Silicon Photo-Multipliers (SiPM) in Time-of-Flight Applications (2018)

73. Claire Tsagkari – Design, Fabrication and Testing of a Capacitive Sensor Using Delta-Sigma Modulation (2017)
72. Kevin Buck – Fast Transient Digitizer and PCB Interface (2015)
71. Marzieh Sharbat Maleki (2015)
70. Angsuman Roy – Design, Fabrication and Testing of Monolithic Low-Power Passive Sigma-Delta Analog-to-Digital Converters (2015)
69. Daniel Anderson – Design and Implementation of an Instruction Set Architecture and Instruction Execution Unit for the RZ9 Coprocessor System (2014)
68. Jared Gordon – Design and Fabrication of an Infrared Optical Pyrometer ASIC (2013)
67. Justin Butterfield (2012)
66. Adam Johnson – Methods and Considerations for Testing Resistive Memories (2012)
65. Ben Millemon – CMOS Characterization, Modeling, and Circuit Design in the Presence of Random Local Variation (2012)
64. Justin Wood (2012)
63. Chamunda Ndinawe Chamunda (2011)
62. Gary VanAckern – Design Guide for CMOS Process On-Chip 3D Inductors using Thru-Wafer Vias (2011)
61. Lucien Jan Bissey – High-Voltage Programmable Delta-Sigma Modulation Voltage-Control Circuit (2010)
60. Kaijun Li (2010)
59. Yingting Li (co-supervised with Maria Mitkova) (2010)
58. Lael Matthews (co-supervised with Said Ahmed-Zaid) (2010)
57. Priyanka Mukeshbhai Parikh (2010)
56. Todd Plum (co-supervised with Jeff Jessing) – Design and Fabrication of a Chemicapacitive Sensor for the Detection of Volatile Organic Compounds (2010)
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54. Avani Falgun Trivedi (2010)
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52. Mahesh Balasubramanian – Phase Change Memory - Array Development and Sensing Circuits using Delta-Sigma Modulation (2009)
51. Lincoln Bollschweiler (2009)
50. Shantanu Gupta (2009)
49. Qawi Harvard – Wide I_O DRAM Architecture Utilizing Proximity Communication (2009)
48. Avinash Rajagiri (2009)
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43. Curtis Cahoon – Low-Voltage CMOS Temperature Sensor Design using Schottky Diode-Based References (2008)
42. Prashanth Busa (2008)
41. John McCoy III (2008)
40. Dennis Montierth – Using Delta-Sigma-Modulation for Sensing in a CMOS Imager (2008)
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38. Barsha Shrestha (co-supervised with Zhu Han) – Wireless Access in Vehicular Environments using Bit Torrent and Bargaining (2008)
37. Eric Becker – Design of an Integrated Half-Cycle Delay Line Duty Cycle Corrector Delay Locked Loop (2007)
36. Matthew Leslie – Noise-Shaping Sense Amplifier for Cross-Point Arrays (2007)
35. Jose Monje (2007)
34. Sanghyun Park (2007)
33. Vishal Saxena – Indirect Feedback Compensation Techniques for Multi-Stage Operational Amplifiers (2007)
32. Meshack Appikatla (2006)
31. Eric Booth – Wide Range, Low Jitter Delay-Locked Loop Using a Graduated Digital Delay Line and Phase Interpolator (2006)

30. Sucheta Das (2006)
29. Krishna Duvvada – High Speed Digital CMOS Input Buffer Design (2006)
28. Krishnamraju Kurra (2006)
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26. Roger Porter (2006)
25. David Butler – Low-Voltage Bandgap Reference Design Utilizing Schottky Diodes (2005)
24. Dragos Dimitriu (2005)
23. Surendranath Eruvuru – Sensing Circuit Design for an Ion Mobility Spectrometer (2005)
22. Sandhya Sandireddy (2005)
21. Harish Singidi (2005)
20. Indira Vemula – Delta-Sigma Modulator Used in CMOS Imagers (2005)
19. Bhavana Kollimarla – A 1-Bit Analog-to-Digital Converter Using Delta Sigma Modulation for Sensing in CMOS Imagers (2004)
18. Sandeep Pemmaraju – High Voltage Charge Pump Circuit for an Ion Mobility Spectrometer (2004)
17. Ravindra Puthumbaka – Circuit Design for an Ion Mobility Spectrometer (2004)
16. Brandon Roth – Comparison of Asynchronous vs. Synchronous Design Technologies using a 16-bit Binary Adder (2004)
15. Jennifer Taylor – Reading and Writing Flash Memory Using Delta-Sigma Modulation (2004)
14. Jing Plaisted – Methods for Memory Testing (2003)
13. Murugesh Subramaniam – Flash Memory Sensing Using Averaging (2003)
12. Brian Johnson – Application of an Asynchronous FIFO in a DRAM Data Path (2002)
11. Scott Ward – Electrostatic Discharge (ESD) Protection in CMOS (2002)
10. Tyler Gomm – Design of a Delay-Locked Loop with a DAC-Controlled Analog Delay Line (2001)
9. Gexin Huang (2001)
8. Chris Atkins (2000)
7. Thaddeus Black (2000)
6. Zuxu Qin (2000)
5. Hao Chen (1999)
4. Doug Hackler (co-supervised with Steve Parke) – TMOS: A Novel Design for MOSFET Technology (1999)
3. Song Liu – Design of a CMOS 6-bit Folding and Interpolating Analog-to-Digital Converter (1999)
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144. Baker, R. J., "Quantizing circuits having improved sensing," **9,449,664**, September 20, 2016.
143. Baker, R. J., "Error detection for multi-bit memory," **9,336,084**, May 10, 2016.
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139. Baker, R. J., "Resistive memory element sensing using averaging," **9,081,042**, July 14, 2015.
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117. Baker, R. J., "Integrators for delta-sigma modulators," **8,102,295**, January 24, 2012.
116. Baker, R. J., "Devices including analog-to-digital converters for internal data storage locations," **8,098,180**, January 17, 2012.
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99. Baker, R. J., "Quantizing circuits with variable reference signals," **7,733,262**, June 8, 2010.
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97. Baker, R. J., and Beigel, K. D., "Multi-resistive integrated circuit memory," **7,642,591**, January 5, 2010.
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95. Baker, R. J., "Resistive memory element sensing using averaging," **7,577,044**, Aug. 18, 2009.

94. Baker, R. J., "Quantizing circuits with variable parameters," **7,538,702**, May 26, 2009.
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89. Baker, R. J., "Per column one-bit ADC for image sensors," **7,456,885**, November 25, 2008.
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87. Li, W., Schoenfeld, A., and Baker, R. J., "Method and apparatus for providing symmetrical output data for a double data rate DRAM," **7,421,607**, September 2, 2008.
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- Harvard, Q. I. and Baker, R. J., “Low-Power, High-Bandwidth, and Ultra-Small Memory Module Design,” a presentation covering semiconductor packaging, DRAM architectures, and I/O circuits. The goal of this work is to investigate replacing the currently used dual in-line memory modules (DIMMs) with a smaller and a lower power memory module, a “Nano-Module.”
- Baker, R. J., and Campbell, K. A., “Reconfigurable Analog Electronics using the Memristor.”
- Baker, R. J., and Saxena, V., “A K-Delta 1-Sigma Modulator for Wideband Analog-to-Digital Conversion.”
- Li, K., Saxena, V., and Baker, R. J., "The Baker ADC: An Overview,"
- Saxena, V., and Baker, R. J., "High-Speed Op-Amp Design: Compensation and Topologies for Two and Three Stage Designs,"
- Baker, R. J., "Circuit Design for MLC Flash: Towards a Semiconductor Replacement for the Hard Disk Drive."
- Baker, R. J., Terman Award Acceptance Speech, given at the Frontiers in Education Conference (FIE 2007), Milwaukee, WI, October 11, 2007.
- Baker, R. J., "The One-Transistor, One-Capacitor (1T1C) Dynamic Random Access Memory (DRAM), and its Impact on Society," presented at the Franklin Institute, in the symposium honoring Dr. Robert H. Dennard and his receipt of the 2007 Benjamin Franklin Medal in Electrical Engineering, April 25, 2007.
- Baker, R. J. and Saxena, V., "Design of Bandpass Delta-Sigma Modulators: Avoiding Common Mistakes."
- Baker, R. J., "Sensing Circuits for Resistive Memory."
- Hadrick, M. and Baker, R. J., "Sensing in CMOS Imagers using Delta-Sigma Modulation."

- Baker, R. J., "Design of High-Speed CMOS Op-Amps for Signal Processing," IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED), April, 2005
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14. Lawrence, C.E., Cheek, B. J., Lawrence, T. E., Kumar, S., Haggag, A., Baker, R. J., and Knowlton, W. B., *Gate Dielectric Degradation Effects on nMOS Devices Using a Noise Model Approach*, IEEE University/Government/Industry Microelectronics (UGIM) Symposium, June 30 - July 2, 2003.
13. Cheek, B., Lawrence, C., Lawrence, T., Gomez, J., Caldwell, T., Kiri, D., Kumar, S., Baker, R. J., Moll, A. J., and Knowlton, W. B., *Gate Dielectric Degradation Effects on nMOS Devices and Simple IC Building Blocks (SICBBs),* IEEE Electron Devices Society Boise Meeting, Boise, ID Oct. 25, 2002.
12. Lawrence, C., Cheek, B., Caldwell, T., Lawrence, T., Kiri, D., Kumar, S., Baker, R. J., Moll, A. J., and Knowlton, W. B., *Pulse voltage stressing of ultrathin gate oxides in NMOS devices, poster session at IEEE International Integrated Reliability Workshop,* October 21-24, 2002.
11. Cheek, B., Lawrence, C., Lawrence, T., Caldwell, T., Kiri, D., Kumar, S., Baker, R. J., Moll, A. J., and Knowlton, W. B., Circuit level reliability of ultrathin gate oxides for SICBBs: Preliminary study concentrated on the effect of stress on the NMOSFET of an inverter, poster session at the IEEE International Integrated Reliability Workshop, October 21-24, 2002.
10. Baker, R. J., "Sensing Circuits for Resistive Memory," *IEEE Electron Devices Society* Meeting, Boise, Idaho October 25, 2002.
9. Rivera, B., Baker, R. J., Melngailis, J., "Design and Layout of Schottky Diodes in a Standard CMOS Process," 2001 International Semiconductor Device Research Symposium, Washington DC, Dec. 2001.
8. Hess, H. and Baker, R. J., "Easier Method to Simultaneously Trigger Series-Connected MOS Devices," *Power Systems World Conference* 2000, Boston, Massachusetts, September 2000.
7. Baker, R. J., and Hess, H., "Transformerless Capacitive Coupling of Gate Signals for Series Operation of Power MOSFET Devices." *International Electric Machines and Drives Conference,* Seattle, Washington, May 1999, pp. 673-676.
6. Baker, R. J., "A windows based integrated circuit design tool for distance education," *International Conference on Simulation and Multimedia in Engineering Education*."
5. Chen, H. and Baker, R. J., "A CMOS Standard-Cell Library for the PC-based LASI Layout System," *Proceedings of the 41st International Midwest Symposium on Circuits and Systems, August 9-12, 1998.*
4. Liu, S. and Baker, R. J., "Process and temperature performance of a CMOS beta-multiplier voltage reference," *Proceedings of the 41st International Midwest Symposium on Circuits and Systems, August 9-12, 1998.*
3. Boyce, D.E. and Baker, R. J., "A Complete Layout System for the PC," *IEEE 40th International Midwest Symposium on Circuits and Systems*, 1997.
2. Baker, R. J., and Blair, J. J., "Step response considerations and the design of a suitable step generator for high speed digitizer testing," *LLNL's Third Annual Workshop on High Speed Digitizers,* April 3-4, Las Vegas, Nevada, 1991.
1. Baker, R. J., "Step-recovery diodes sharpen pulses," *Engineering Design News Magazine*, pp. 154-156, May 10, 1990.

EXPERT WITNESS EXPERIENCE

The law firms and clients (underlined) whom I have provided expert witness services in electrical and computer engineering are listed below. I have been deposed 108 times, given expert testimony at 14 trials (7 USITC, 2 D. Del., 1 Arbitr., 1 S.D. Cal., 1 N.D. Ga., 1 D. Ore., and 1 E.D. Tex.), and participated in 1 mediation.

Pillsbury Winthrop Shaw Pittman LLP (San Francisco, CA)

Case – *MediaTek, Inc.* v. Redstone Logics LLC
Case Number – IPR2025-00085. Petition filed on October 22, 2024.
Case Subject Matter – multi-core processors with voltage and clock scaling functionality and related communications/control signaling.
Work Performed – Provided expert consulting services for inter partes reviews and wrote declaration.

Baker Botts LLP (Houston, TX)

Case – *Innolux Corporation* v. Phenix Longhorn LLC

Case Numbers – IPR2025-00043 and IPR2025-00044. Petitions filed on October 15, 2024.

Case Subject Matter – Systems and methods for outputting “corrected” gamma reference voltages to drive a Liquid Crystal Display (LCD).

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Baker Botts LLP (Austin, TX and Houston, TX)

Case – *Silicon Motion Inc.* v. K.Mizra, LLC

Case Number – IPR2024-01236. Petition filed on September 10, 2024.

Case Number – IPR2024-01240. Petition filed on August 13, 2024.

Case Number – IPR2024-01241. Petition filed on August 9, 2024.

Case Subject Matter – Calibrating a memory controller for use with DDR (double-data rate) DRAM (dynamic random access memory). Calibrating a communication channel to receive a digital signal. A micro-threaded memory device.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Garlick & Markison, LLC (Phoenix, AZ and Austin, TX)

Case – Ex Parte Reexamination

Case Number – 90/019612. Request filed on August 6, 2024.

Case Subject Matter – Semiconductor manufacturing processes, fabrication and packaging of integrated circuits, layout and routing of signal lines.

Work Performed – Provided expert consulting services and wrote declaration.

Bookoff McAndrews, PLLC (Washington, DC)

Case – *Lenovo Inc.* v. Intellectual Ventures II LLC

Case – *Lenovo Inc.* v. University of Rochester

Case Numbers – IPR2024-01225 and IPR2024-01226. Petitions filed on August 2, 2024.

Case Subject Matter – Methods for calibrating intra-cycle timing in digital communications. Digital circuits with multiple clock domains.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

DLA Piper LLP (Palo Alto, CA and Austin, TX)

Case – *BOE Technology Group Co., Ltd.* v. Optronic Sciences LLC

Case Numbers – IPR2024-01130, IPR2024-01133, and IPR2024-01134. Petitions filed on July 5, 2024

Case Subject Matter – Imaging pixels, layout, and fabrication. Light emitting devices, including packaging, covers, and structures.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Dentons US LLP (Washington, DC)

Case – *Reolink Digital Technology Co., Ltd.* v. KT Imaging US, LLC

Case Numbers – IPR2024-01154 and IPR2024-01155. Petitions filed on July 3, 2024

Case Subject Matter – Image sensor structure and package with integrated lens module for digital image products such as digital cameras, camera phones, video phones, fingerprint readers and so on.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Paul Hastings LLP (Washington, DC)

Case – Ex Parte Reexaminations

Case Numbers – 90/019,560, 90/019,962, and 90/019,964. Requests filed on July 1, 2024

Case Numbers – 90/019,556, 90/019,557, and 90/019,558. Requests filed on June 28, 2024.

Case Subject Matter – Wireless charging systems, power sources, and inductive receivers for charging mobile devices.

Work Performed – Provided expert consulting services and wrote declarations for ex parte reexaminations.

Banner Witcoff (Chicago, IL and Washington, DC)

Case – *ZF Friedrichshafen AG, ZF Active Safety and Electronics US LLC, and Nissan Motor Company, Ltd.* v. Foras Technologies, Ltd.

Case Number – IPR2024-00969. Petition filed on June 24, 2024.

Case Subject Matter – Detecting loss of lockstep between pairs of processors and loss of lockstep recovery

Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Fish & Richardson P.C. (San Diego, CA and Boston, MA)

Case – *Vicor Corporation* v. Delta Electronics, Inc.

Case Numbers – IPR2024-00704, IPR2024-00705, IPR2024-00706, and IPR2024-00715. Petitions filed on March 25, 2024.

Case Subject Matter – Power converters including design, packaging, heatsinking and manufacturing. Resonant converters with overcurrent protection.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Mintz, Levin, Cohn, Ferris, Glovsky and Popeo, P.C. (Boston, MA)

Case – RoadRunner Recycling, Inc. v. *Recycle Tract Systems*

Case Number – California, ND 3:23-cv-04804. Amended complaint filed on January 16, 2024.

Case Subject Matter – Waste and recycling metering technology.

Work Performed – Provided expert consulting services including writing expert report. Was deposed.

Winston & Strawn LLP (Los Angeles, CA and Redwood City, CA)

Case – *Silicon Motion, Inc.* v. Unification Technologies LLC

Case Number – IPR2024-00199. Petition filed on December 18, 2023.

Case Subject Matter – Memory controller, solid-state drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Garlick & Markison, LLC (Austin, TX)

Case – *NXP USA, Inc.* v. Bell Semiconductor, LLC

Case Numbers – IPR2024-00167 and IPR2024-00168. Petitions filed on November 9, 2023.

Case Subject Matter – Semiconductor manufacturing processes, fabrication and packaging of integrated circuits, layout and routing of signal lines.

Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed.

Unified Patents, LLC (Washington, DC)

Case – Ex Parte Reexamination

Case Number – 90/019288. Request filed on October 20, 2023.

Case Subject Matter – Power conversion device to drive an alternating-current motor for an electric vehicle.

Work Performed – Provided expert consulting services and wrote declaration.

Haynes and Boone, LLP (Dallas, TX)

Case – *Western Digital Technologies, Inc.* v. Longitude Licensing LTD.

Case Number – IPR2023-01200. Petition filed on July 14, 2023.

Case Subject Matter – Communications between a memory controller and memory.

Work Performed – Provided expert consulting services, wrote declaration for inter partes review, and was deposed.

Paul Hastings LLP (Washington, DC)

Case – *Samsung Electronics Co., Ltd.* v. Mojo Mobility, Inc.

Case Numbers – IPR2023-01094, IPR2023-01095, IPR2023-01096, IPR2023-01097, IPR2023-01098, IPR2023-01099, IPR2023-01100, and IPR2023-01124. Petitions filed on June 30, 2023.

Case Numbers – IPR2023-01101 and IPR2023-01102. Petitions filed on June 29, 2023.

Case Numbers – IPR2023-01091, IPR2023-01092, and IPR2023-01093. Petitions filed on June 28, 2023.

Case Numbers – IPR2023-01086, IPR2023-01087, IPR2023-01088, IPR2023-01089, and IPR2023-01090. Petitions filed on June 27, 2023.

Case Subject Matter – Wireless charging systems, power sources, and inductive receivers for charging mobile devices.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Winston & Strawn LLP (Los Angeles, CA, Redwood City, CA, Chicago, IL, and Houston, TX)

Case – Unification Technologies LLC v. *Silicon Motion, Inc.*

Case Number – Texas, ED (Marshall) 2:23-cv-00267. Complaint filed June 2, 2023.

Case Subject Matter – Memory controller, solid-state drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services.

Norton Rose Fulbright LLP (Austin, TX and Dallas, TX)

Case – *Current Lighting Solutions, LLC d/b/a GE Current* v. Jiaxing Super Lighting Electric Appliance Co., Ltd.

Case Numbers – IPR2023-00979 and IPR2023-00980. Petitions filed on May 31, 2023.

Case Number – IPR2023-00270. Petition filed on December 19, 2022.

Case Number – IPR2023-00271. Petition filed on December 14, 2022.

Case Subject Matter – LED lighting, lamps, tube lamps, assembly, and associated circuits and electronics.

Work Performed – Provided expert consulting services and wrote declarations for inter partes review.

Faegre Drinker Biddle & Reath LLP (San Francisco, CA, Washington, DC, and Minneapolis, MN)

Case – CogniPower LLC v. *Samsung Electronics*

Case Number – Texas, ED (Marshall) 2:23-cv-00160. Complaint filed April 10, 2023.

Case Subject Matter – Power conversion using switching power supplies.

Work Performed – Provided expert consulting services and wrote expert reports.

Baker Botts LLP (Dallas, TX)

Case – *Lennox Industries Inc.* v. Rosen Technologies LLC

Case Numbers – IPR2023-00715, IPR2023-00716, IPR2023-00717, IPR2023-00718, and IPR2023-00719. Petitions filed on March 29, 2023.

Case Subject Matter – Thermostat system communications, programming, and displays.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Cooley LLP (Palo Alto, CA)

Case – *Nintendo Co., Ltd. and Nintendo of America Inc.* v. Polaris PowerLED Technologies, LLC

Case Number – IPR2023-00778. Petition filed on March 28, 2023.

Case Subject Matter – Visual displays, circuit design, and related technologies.

Work Performed – Provided expert consulting services, wrote declaration for inter partes review, and was deposed.

Bracewell LLP (New York, NY and Seattle, WA)

Case – *Kioxia America, Inc. and Kioxia Corporation* v. BiTMICRO LLC

Case Numbers – IPR2023-00741, IPR2023-00742, and IPR2023-00743. Petitions filed on March 23, 2023.

Case Subject Matter – Solid-state storage devices utilizing multi-profile memory controllers. Optimizing memory operations in a memory system suitable for use in an electronic storage device. Supplying energy to a cache memory using a super capacitor.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Bookoff McAndrews, PLLC (Washington, DC)

Case – *Lenovo Inc. and Motorola Mobility LLC* v. Theta IP, LLC

Case Numbers – IPR2023-00694, IPR2023-00697, and IPR2023-00698. Petitions filed on March 7, 2023.

Case Subject Matter – Power in wireless communication circuits.

Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed.

Sheppard, Mullin, Richter & Hampton LLP (Menlo Park, CA and San Diego, CA)

Case – Semiconductor Design Technologies LLC v. *Cadence Design Systems, Inc.*

Case Number – California, ND 3:23-cv-01001. Complaint filed March 6, 2023.

Case Subject Matter – Semiconductor design support device/method and manufacturing method for semiconductor integrated circuit.

Work Performed – Provided expert consulting services.

McDermott Will & Emery LLP (Chicago, IL and Austin, TX)

Case – *Xilinx, Inc.* v. Polaris Innovations Limited

Case Numbers – IPR2023-00513 and IPR2023-00514. Petitions filed on February 6, 2023.

Case Subject Matter – Methods for terminating a memory chip with various termination resistances and output drivers for integrated circuits.

Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed.

Willkie Farr & Gallagher LLP (San Francisco, CA)

Case –Bell Semiconductor, LLC. v. *Synopsys, Inc.*

Case Number – California, SD 3:22-cv-00594. Complaint filed on January 31, 2023.

Case Subject Matter – Integrated circuit design computer-aided design (CAD) tools for routing, design rule checking, layout versus schematic, electrical checking, dummy fill, reducing capacitance.

Work Performed – Provided expert consulting services and wrote expert reports.

Fish & Richardson P.C. (Washington, DC, Atlanta, GA, and Boston, MA)

Case – Element Capital Commercial Company PTE. LTD v. *BOE Technology Group Co. LTD and Motorola (Wuhan) Mobility*

Case Number – Texas, ED (Marshall) 2:22-cv-00118. Complaint filed January 11, 2023.

Case Subject Matter – Display technology, layout, circuit design, pixel design and fabrication.

Work Performed – Provided expert consulting services, wrote expert reports, and was deposed.

Baker Botts LLP (San Francisco, CA and New York, NY) and O'Melveny & Myers LLP (Los Angeles, CA)

Case – Polaris PowerLED, LLC v. *Samsung Electronics and Samsung Display*

Case Number – Texas, ED (Marshall) 2:22-cv-00469. Complaint filed December 12, 2022.

Case Subject Matter – active matrix organic light-emitting diode (AMOLED) displays, controlling the intensity of light-emitting diodes in backlights of displays, control circuits for adjusting current delivery based upon temperature.

Work Performed – Provided expert consulting services including writing a declaration for claim construction.

Arnold & Porter (Los Angeles and Palo Alto, CA) and Willkie Farr & Gallagher LLP (San Francisco, CA)

Case – *Synopsys, Inc. and Cadence Design Systems, Inc.* v. Bell Semiconductor, LLC.

Case Number – Delaware, 1:22-cv-01512. Complaint filed on November 18, 2022.

Case Subject Matter – Integrated circuit design computer-aided design (CAD) tools for routing, design rule checking, layout versus schematic, electrical checking, dummy fill, reducing capacitance.

Work Performed – Provided expert consulting services, wrote expert reports, and was deposed.

Paul Hastings LLP (Washington, DC)

Case – Ex Parte Reexaminations
Case Numbers – 90/015155 and 90/015156. Requests filed on November 7, 2022.
Case Number – 90/015134. Request filed on October 14, 2022.
Case Number – 90/015130. Request filed on September 30, 2022.
Case Subject Matter – Packaging and fabrication of light emitting diodes (LEDs).
Work Performed – Provided expert consulting services and wrote declaration.

Russ August & Kabat (Los Angeles, CA)

Case – *Resonant Systems, Inc.* v. Sony
Case Number – Texas, ED (Marshall) 2:22-cv-00424. Complaint filed on October 26, 2022.
Case Subject Matter – Linear vibration modules and linear-resonant vibration modules.
Work Performed – Provided expert consulting services, wrote claim construction disclosure, wrote expert reports, and was deposed.

Sheppard, Mullin, Richter & Hampton LLP (Menlo Park, CA and San Diego, CA) and Willkie Farr & Gallagher LLP (San Francisco, CA)

Case – Bell Semiconductor, LLC v. *NXP*, SMC, Micron, Nvidia, *Advanced Micro Devices (AMD)*, *Acer*, Infineon, Qualcomm, Motorola Mobility, and Western Digital
Case Number – ITC Investigation No. 337-TA-1340. Complaint filed October 6, 2022.
Case Subject Matter – Electronic devices, semiconductor devices, and components.
Work Performed – Provided expert consulting services.

O'Melveny & Myers LLP (Los Angeles, CA)

Case – Daedalus Prime LLC v. *Samsung Electronics* and Qualcomm Inc.
Case Number – ITC Investigation No. 337-TA-1335. Complaint filed September 12, 2022.
Case Subject Matter – Semiconductor devices, mobile devices, and components.
Work Performed – Provided expert consulting services.

Fish & Richardson P.C. (Boston, MA, Houston, TX, and Washington, DC)

Case – Sonrai Memory LTD. v. *Micron Technology, Inc.*
Case Number – Texas, WD (Waco) 6:22-cv-00855 and Texas, WD (Waco) 1:23-cv-01407. Complaint filed August 16, 2022.
Case Subject Matter – Portable RAM drive and variable charge pump circuit with dynamic load.
Work Performed – Provided expert consulting services, wrote expert reports, and was deposed.

Russ August & Kabat (Los Angeles, CA and New York, NY)

Case – *NextGen Innovations, LLC* v. Infinera, Fujitsu, AT&T, and Nokia
Case Number – Texas, ED (Marshall) 2:22-cv-00306, Texas, ED (Marshall) 2:22-cv-00307, Texas, ED (Marshall) 2:22-cv-00308, and Texas, ED (Marshall) 2:22-cv-00309. Complaints filed on August 9, 2022.
Case Subject Matter – optical transmission systems including optical components for encoding, transmission (fiber optic transmitters and receivers), and decoding of data and related standards and concepts.
Work Performed – Provided expert consulting services, wrote claim construction disclosure, wrote expert reports, and was deposed twice.

DLA Piper (Chicago, IL and Washington, DC)

Case – Ampt, LLC v. *SolarEdge Technologies, Inc.*
Case Number – ITC Investigation No. 337-TA-1327. Complaint filed July 28, 2022.
Case Subject Matter – Solar power optimizers, inverters, and components.
Work Performed – Provided expert consulting services including writing declarations for claim construction, expert reports, and was deposed.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, and Irvine, CA)

Case – Signify North America Corporation v. *Shenzhen Intellirocks Tech Co.*
Case Number – Texas, WD (Waco) 6:22-cv-00760. Complaint filed on July 8, 2022.
Case Subject Matter – LED packaging, circuits, and systems.
Work Performed – Provided expert consulting services including writing declaration for claim construction. Was deposed.

Baker Botts LLP (Dallas, TX)

Case – Rosen Technologies LLC v. *Lennox Industries Inc.*
Case Number – Texas, ND (Dallas) 3:22-cv-00732. Complaint filed on June 7, 2022.
Case Subject Matter – Thermostat system communications, programming, and displays.
Work Performed – Provided expert consulting services.

Paul Hastings LLP (Austin, TX and Washington, DC)

Case – *Samsung Electronics Co., Ltd.* v. Scramoge Technology Ltd.
Case Numbers – IPR2022-01052, IPR2022-01053, and IPR2022-01058. Petitions filed on May 26, 2022.
Case Numbers – IPR2022-01054, IPR2022-01055, IPR2022-01056, and IPR2022-01057. Petitions filed on May 24, 2022.
Case Number – IPR2022-00939. Petition filed on April 29, 2022.
Case Subject Matter – An antenna that supports wireless charging using switching power supplies such as flyback converters.
Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, Irvine, CA, and Menlo Park, CA)

Case – Ex Parte Reexaminations
Case Number – 90/015020. Request filed on May 2, 2022.
Case Number – 90/014906. Request filed on November 12, 2021.
Case Number – 90/014899. Request filed on November 10, 2021.
Case Number – 90/014888. Request filed on October 21, 2021.
Case Numbers – 90/014886 and 90/014887. Requests filed on October 20, 2021.
Case Number – 90/014885. Request filed on October 19, 2021.
Case Subject Matter – Universal Serial Bus (USB) for charging.
Work Performed – Provided expert consulting services and wrote declarations**.**

DLA Piper (Chicago, IL, Austin, TX, and Washington, DC)

Case – *SolarEdge Technologies, Inc.* v. Fronius International GMBH
Case Number – IPR2022-00849. Petition filed on April 14, 2022.
Case Subject Matter – Mechanical assembly and enclosure whereby an upper housing part is detached from a lower housing part using a “rotate-and-lift” feature.
Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Kirkland & Ellis LLP (New York, NY)

Case – *Samsung Electronics Co.* v. Sonrai Memory Ltd.
Case Numbers – IPR2022-00305 and IPR2022-00306. Petitions filed on December 10, 2021.
Case Subject Matter – USB devices and circuits for saving power.
Work Performed – Provided expert consulting services including writing declarations for inter partes reviews.

Haynes and Boone, LLP (Washington, DC)

Case – *Unified Patents, LLC* v. Arigna Technology Limited
Case Number – IPR2022-00285. Petition filed on December 9, 2021.
Case Subject Matter – High voltage driver circuit for driving power devices such as insulated gate bipolar transistors (IGBTs).
Work Performed – Provided expert consulting services, wrote declaration for inter partes review and was deposed.

Paul Hastings LLP (Washington, DC)

Case – *Samsung Electronics Co., Ltd.* v. Lynk Labs, Inc.

Case Numbers – IPR2022-00149 and IPR2022-00150. Petitions filed on November 12, 2021

Case Numbers – IPR2022-00100 and IPR2022-00101. Petitions filed on October 28, 2021.

Case Numbers – IPR2022-00051, IPR2022-00052, and IPR2022-00098. Petitions filed on October 27, 2021.

Case Numbers – IPR2021-01575 and IPR2021-01576. Petitions filed on October 1, 2021.

Case Numbers – IPR2021-01299, IPR2021-01300, IPR2021-01345, IPR2021-01346, and IPR2021-01347. Petitions filed on September 7, 2021.

Case Subject Matter – Circuit design, including switching power supply design (e.g., flyback), rectifiers, power factor correction, etc. for lighting and displays using light emitting diodes (LEDs).

Work Performed – Provided expert consulting services, wrote declarations, and was deposed ten times.

Haynes and Boone, LLP (Plano, TX)

Case – *Pure Storage, Inc.* v. Digital Cache, LLC

Case Number – IPR2022-00121. Petition filed on October 29, 2021.

Case Subject Matter – Non-volatile memory (NVM) devices capable of retaining stored data in case of a power failure.

Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Banner Witcoff (Washington, DC)

Case – *SolarEdge Technologies Ltd.* v. Koolbridge Solar, Inc.

Case Numbers – IPR2022-00007, IPR2022-00008, IPR2022-00009, IPR2022-00010, IPR2022-00011, and IPR2022-00012. Petitions filed on October 11, 2021.

Case Numbers – IPR2022-00013, IPR2022-00014, and IPR2022-00015. Petitions filed on October 8, 2021.

Case Subject Matter – DC-to-AC converters using full-bridges, multi-level conversion for power systems, and other electronics for harvesting solar energy.

Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed.

Paul Hastings LLP (Austin, TX and Washington, DC)

Case – *Samsung Electronics Co., Ltd.* v. LED Wafer Solutions LLC

Case Number – IPR2021-01554. Petition filed on September 20, 2021.

Case Number – IPR2021-01526. Petition filed on September 10, 2021.

Case Number – IPR2021-01506. Petition filed on September 7, 2021.

Case Number – IPR2021-01491. Petition filed on September 3, 2021.

Case Subject Matter – Packaging of light emitting diodes (LEDs).

Work Performed – Provided expert consulting services and wrote declarations.

Paul Hastings, LLC (Washington, DC)

Case – Ex Parte Reexamination

Case Number – 90/014,846. Request filed on August 30, 2021.

Case Subject Matter – Wireless power transmission and ways to wirelessly charge and/or discharge a battery.

Work Performed – Provided expert consulting services and wrote declaration.

Jones Day (San Diego, CA and Pittsburgh, PA)

Case – *SOLiD, Inc.* v. CommScope Technologies LLC

Case Numbers – IPR2021-01390, IPR2021-01391, IPR2021-01392, IPR2021-01393, and IPR2021-01394. Petitions filed on August 12, 2021.

Case Subject Matter – Digital antenna system that enables extension of radio frequency (RF) analog signals from base stations to areas (e.g., inside of buildings) where access to such signals is inhibited.

Work Performed – Provided expert consulting services for inter partes reviews and wrote declaration.

Unified Patents, LLC (Washington, DC)

Case – Ex Parte Reexamination
Case Number – 90/019,015. Request filed on July 20, 2021.
Case Subject Matter – Voltage-controlled oscillator (VCO) temperature compensation.
Work Performed – Provided expert consulting services and wrote declaration.

Winston & Strawn LLP (Dallas, TX and Palo Alto, CA)

Case – *Micron Technology, Inc.; Micron Semiconductor Products, Inc.; Micron Technology Texas LLC* v. Unification Technologies LLC
Case Numbers – IPR2021-00940, IPR2021-00941, and IPR2021-00942. Petitions filed on June 4, 2021.
Case Subject Matter – Solid-State Drive (SSD), flash non-volatile memory management, memory controller operation and addressing.
Work Performed – Provided expert consulting services for inter partes reviews and wrote declarations.

Hill, Kertscher & Wharton, LLP (Atlanta, GA)

Case – Kaijet Technology v. *Sanho Corporation*
Case Number – IPR2021-00886. Petition filed on April 30, 2021.
Case Subject Matter – Port extension apparatus for headphone jack, USB (Universal Serial Bus or Type-C ports), and video ports such as VGA (Video Graphics Array), DVI (Digital Visual Interface), HDMI (High-Definition Multimedia Interface), DP (Display Port), and mini-DP.
Work Performed – Provided expert consulting services for inter partes review, wrote declaration, was deposed.

O'Melveny & Myers LLP (Los Angeles, CA and New York, NY)

Case – Solas OLED LTD. v. *Samsung Electronics Co. LTD.*
Case Number – Texas, ED (Marshall) 2:21-cv-00105. Complaint filed March 22, 2021.
Case Subject Matter – Touch-sensors for gesture recognition and signal processing for capacitive touch displays.
Work Performed – Provided expert consulting services including writing declaration for claim construction.

O'Melveny & Myers LLP (San Francisco, CA)

Case – Super Interconnect Technologies LLC v. *Google LLC*
Case Number – Texas, ED (Marshall) 2:18-cv-00463 (complaint filed November 2, 2018) and Texas, WD (Waco) 6:21-cv-00259 (complaint filed March 15, 2021).
Case Subject Matter – Transmission of data and clock signals. Serial signals such as transition minimized differential signaling. Communications between processors and non-volatile storage such as Universal Flash Storage (UFS) and embedded MultiMedia Controller (eMMC).
Work Performed – Provided expert consulting services and wrote expert reports.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, and Irvine, CA)

Case – Fundamental Innovation Systems International LLC v. *Anker Innovations and Fantasia Trading LLC d/b/a Ankerdirect*
Case Number – Delaware, 1:21-cv-00339. Complaint filed on March 5, 2021.
Case Subject Matter – Universal Serial Bus (USB) for charging mobile devices.
Work Performed – Provided expert consulting services, wrote expert reports, and was deposed.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, Irvine, CA, and Menlo Park, CA)

Case – *TCT Mobile Inc. and TCL Communication, Inc.* v. Fundamental Innovation Systems International LLC
Case Numbers – IPR2021-00597, IPR2021-00598, and IPR2021-00599. Petitions filed on February 26, 2021.
Case Number – IPR2021-00428. Petition filed on January 13, 2021.
Case Number – IPR2021-00410. Petition filed on January 11, 2021.
Case Number – IPR2021-00395. Petition filed on December 31, 2020.
Case Subject Matter – Universal Serial Bus (USB) for charging mobile devices.
Work Performed – Provided expert consulting services including writing declarations for inter partes reviews. Was deposed twice.

Paul Hastings LLP (Austin, TX and Washington, DC)

Case – *Samsung, Inc.* v. Pictos Technologies, Inc.
Case Number – IPR2021-00557. Petition filed on February 18, 2021.
Case Number – IPR2021-00436. Petition filed on January 19, 2021.
Case Numbers – IPR2021-00437 and IPR2021-00438. Petitions filed on January 15, 2021.
Case Subject Matter – Solid-state imaging devices including red, green, and blue pixels, data conversion circuits, and interpolation circuits. CMOS imagers including fabrication and design, active pixels, and semiconductor physics.
Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

O'Melveny & Myers LLP (San Francisco, CA) and DLA Piper (New York, NY)

Case – Solas OLED Ltd. v. *BOE Technology Group Co. Ltd. and Samsung Electronics*
Case Number – ITC Investigation No. 337-TA-1243. Complaint filed January 5, 2021.
Case Subject Matter – Active matrix OLED display devices and components
Work Performed – Provided expert consulting services, wrote expert reports, was deposed, and testified at trial.

Paul Hastings LLP (Washington, DC)

Case – *Samsung, Inc.* v. Garrity Power Services LLC
Case Number – IPR2021-00389. Petition filed on December 31, 2020.
Case Subject Matter – Power electronics including full-bridge PWM modules for wireless power transmission using magnetic coupling via antennas and transformers. Design of inductors and coils.
Work Performed – Provided expert consulting services and wrote declaration for inter partes reviews.

Morgan, Lewis & Bockius LLP (Palo Alto, CA and Shanghai, CN)

Case – Monolithic Power Systems, Inc. v. *Meraki Integrated Circuit Technology, Inc. and Promate Electronic Company, LTD.*
Case Number – Texas, WD (Waco) 6:20-cv-00876. Complaint filed on December 24, 2020.
Case Subject Matter – Design of switching power supplies including synchronous rectification.
Work Performed – Provided expert consulting services including declaration for claim construction, trade secret analysis and declaration, and Markman tutorial.

Winston & Strawn LLP (Dallas, TX and Palo Alto, CA)

Case – *Micron Technology, Inc.; Micron Semiconductor Products, Inc.; Micron Technology Texas LLC; Dell Technologies Inc.; Dell Inc.; and HP Inc.* v. Unification Technologies LLC
Case Numbers – IPR2021-00343, IPR2021-00344, and IPR2021-00345. Petitions filed on December 22, 2020.
Case Subject Matter – Solid-State Drive (SSD), flash non-volatile memory management, memory controller operation and addressing.
Work Performed – Provided expert consulting services for inter partes reviews, wrote declarations, and was deposed.

Jones Day (Chicago, IL and Dallas, TX)

Case – WSOU Investments, LLC d/b/a Brazos Licensing and Development v. *Xilinx, Inc.*
Case Numbers – Delaware, 1:20-cv-01231 and Delaware, 1:20-cv-01233. Complaints filed on November 23, 2020 and September 16, 2020.
Case Subject Matter – Controlling power cycles in communication devices and transferring multiple asynchronous clock signals.
Work Performed – Provided expert consulting services, wrote claim construction declaration, wrote expert reports, and was deposed.